

S2-Compatible 7-Input 3-Output Audio/Video Switch

Description

The CXA2069Q is a 7-input, 3-output audio/video switch featuring I²C bus compatibility for TVs. This IC has input pins that are compatible with S2 protocol.

Features

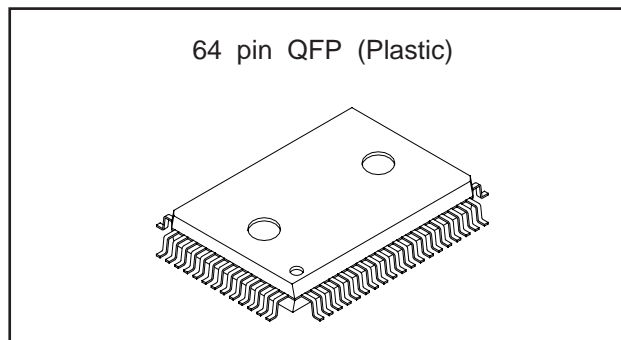
- 4 inputs that are compatible with S2 protocol
- Serial control with I²C bus
- 7 inputs, 3 outputs
- The desired inputs can be selected independently for each of the 3 outputs
- Wide band video amplifier (20 MHz, -3 dB)
- Y/C MIX circuit
- Slave address can be changed (90H/92H)
- Audio muting from external pin
- High impedance maintained by I²C bus lines (SDA, SCL) even when power is OFF
- Wide audio dynamic range (3 V_{rms} typ.)

Applications

Audio/video switch featuring I²C bus compatibility for TVs

Structure

Bipolar silicon monolithic IC



Absolute Maximum Ratings (T_a=25 °C)

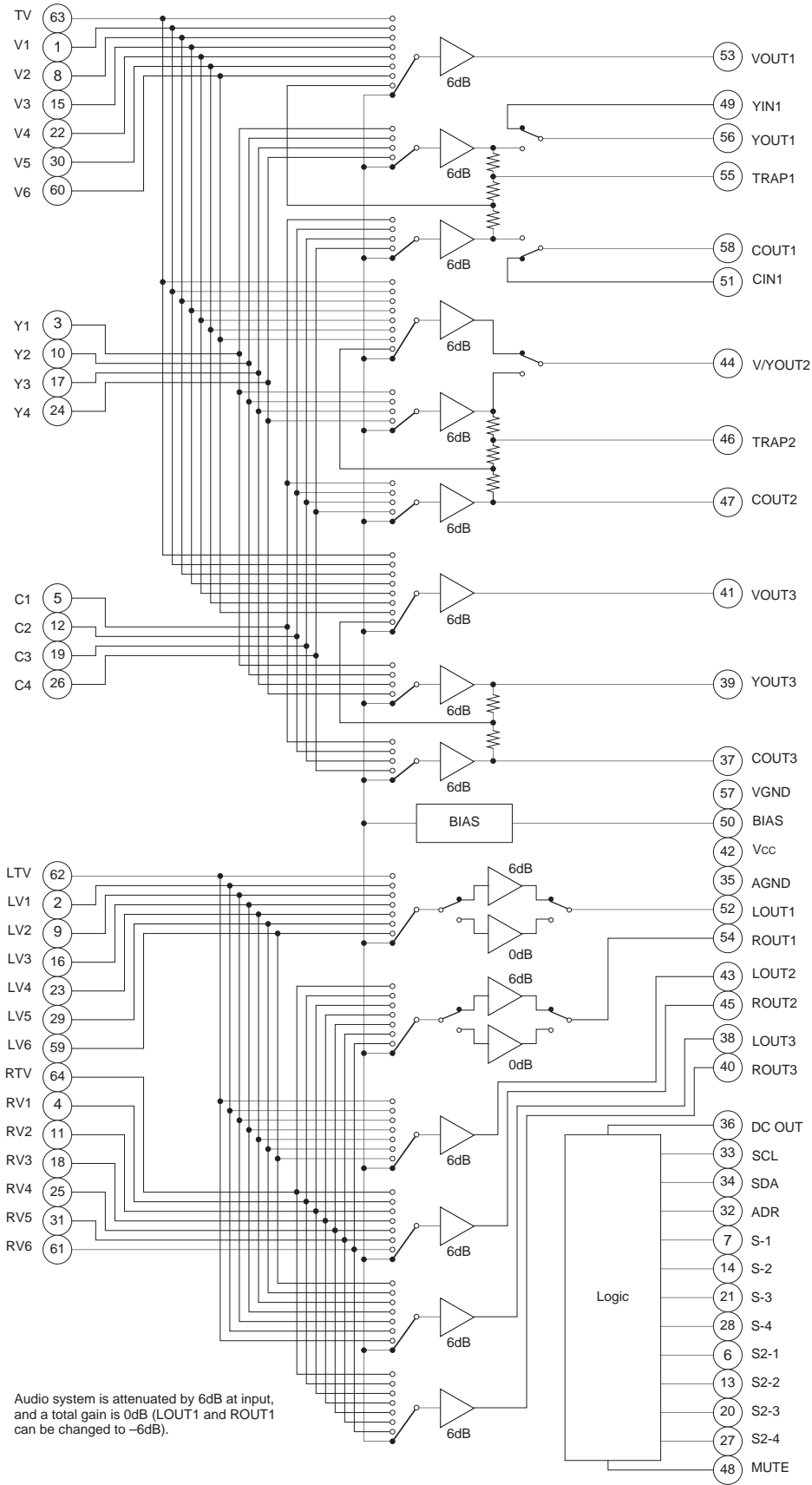
| | | | |
|-------------------------------|------------------|-------------|----|
| • Supply voltage | V _{CC} | 12 | V |
| • Operating temperature | T _{opr} | -20 to +75 | °C |
| • Storage temperature | T _{stg} | -65 to +150 | °C |
| • Allowable power dissipation | P _D | 1300 | mW |

Operating Conditions

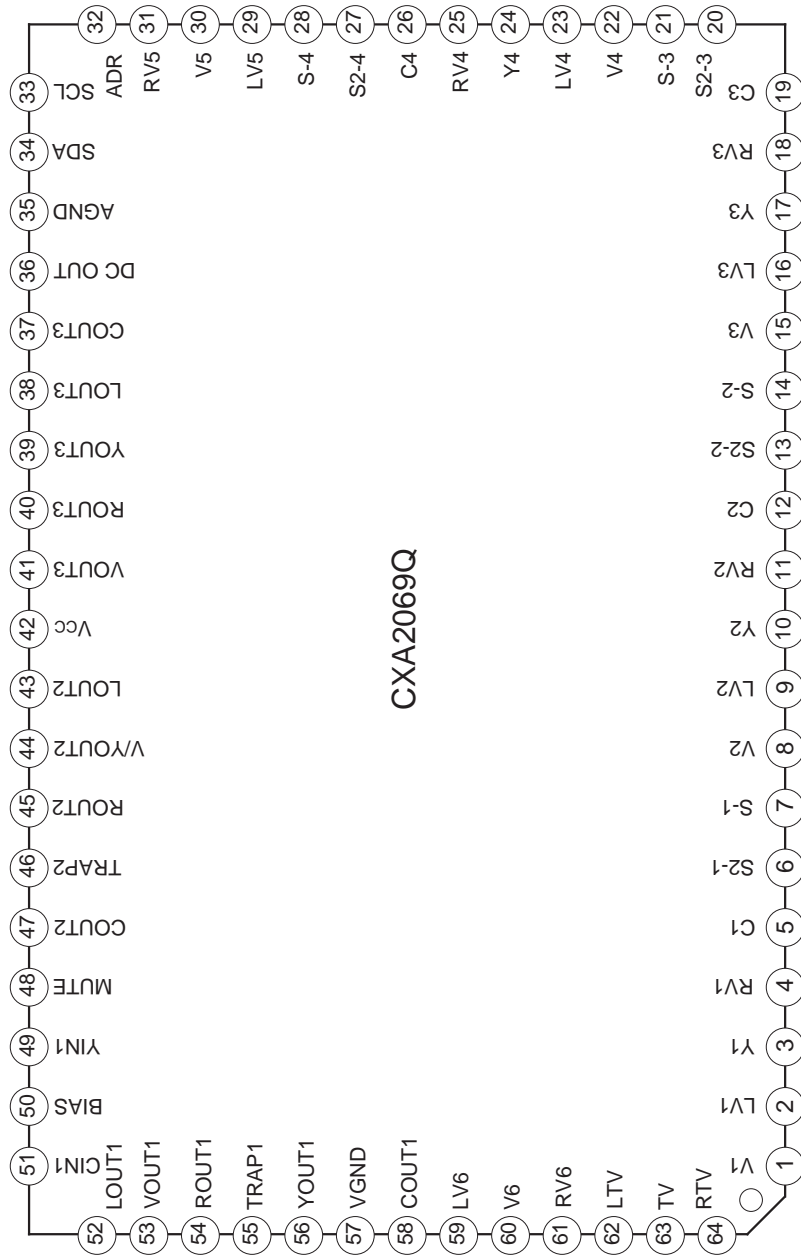
| | | |
|----------------|-------|---|
| Supply voltage | 9±0.5 | V |
|----------------|-------|---|

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Block Diagram



Pin Configuration



CXA2069Q

Pin Description

| Pin No. | Symbol | Pin voltage | Equivalent circuit | Description |
|---|--|-------------|--------------------|--|
| 63 1 8 15 22 30 60 | TV V1 V2 V3 V4 V5 V6 | 4.0 V | | Video signal inputs. Input composite video signals. |
| 3 10 17 24 49 | Y1 Y2 Y3 Y4 YIN1 | 4.0 V | | Y/C separation signal inputs. Input luminance signals. The YIN1 pin inputs the signal obtained by Y/C separating the VOUT1 pin output. |
| 5 12 19 26 51 | C1 C2 C3 C4 CIN1 | 4.5 V | | Y/C separation signal inputs. Input chrominance signals. The CIN1 pin inputs the signal obtained by Y/C separating the VOUT1 pin output. |
| 62, 2 9, 16 23, 29 59, 64 4, 11 18, 25 31, 61 | LTV, LV1 LV2, LV3 LV4, LV5 LV6, RTV RV1, RV2 RV3, RV4 RV5, RV6 | 4.5 V | | Audio signal inputs. |
| 53 41 | VOUT1 VOUT3 | 3.9 V | | Video signal outputs. Output composite video signals. |

| Pin No. | Symbol | Pin voltage | Equivalent circuit | Description |
|----------------------------------|--|-------------|--------------------|--|
| 44 | V/YOUT2 | 3.8 V | | Video signal output. Either composite video signal output or luminance signal output can be selected by I ² C bus control. |
| 56 | YOUT1 | 3.3 V | | Video signal outputs. Output luminance signals. |
| 39 | YOUT3 | 3.8 V | | |
| 58 47 37 | COUT1 COUT2 COUT3 | 4.5 V | | Video signal outputs. Output chrominance signals. |
| 52 43 38 54 45 40 | LOUT1 LOUT2 LOUT3 ROUT1 ROUT2 ROUT3 | 4.5V | | Audio signal outputs. Z _o =50 Ω (within DC ±2 mA) |
| 6 13 20 27 | S2-1 S2-2 S2-3 S2-4 | — | | Detects the S2-compatible DC superimposed onto the C signal. 4 : 3 video signal at 1.3 V or less 4 : 3 letter-box signal at 1.3 V or more to 2.5 V or less 16 : 9 picture squeezed signal at 2.5 V or more This pin is pulled down to GND by a 100 kΩ resistor, so the 4 : 3 video signal is selected when open. |

| Pin No. | Symbol | Pin voltage | Equivalent circuit | Description |
|---------------------|--------------------------|-------------|--------------------|--|
| 7 14 21 28 | S-1 S-2 S-3 S-4 | — | | <p>Composite video/S selector. The detection results are written to the status register. S signal at 3.5 V or less Composite video signal at 3.5 V or more This pin is pulled up to 5 V by a 100 kΩ resistor, so the composite video signal is selected when open.</p> |
| 32 | ADR | — | | <p>Selects the slave address for the I²C bus. 90H at 1.5 V or less 92H at 2.5 V or more 90H when open.</p> |
| 33 | SCL | — | | <p>I²C bus signal input V_{ILmax}=1.5 V V_{IHmin}=3.0 V</p> |
| 34 | SDA | — | | <p>I²C bus signal input V_{ILmax}=1.5 V V_{IHmin}=3.0 V V_{OLmax}=0.4 V</p> |

| Pin No. | Symbol | Pin voltage | Equivalent circuit | Description | | | | | | | | | | |
|--------------|----------------|-------------|--------------------|---|--------------|-----------|---|-------|---|-----|---|-------|---|-------|
| 36 | DC_OUT | — | | <p>Outputs the S2-compatible DC superimposed onto the COOUT3 output. The DC is superimposed by connecting this pin to the COOUT3 output via a capacitor.</p> <p>Control is performed by the I²C bus. When 0 V is output, Q1 is ON and the impedance is 5 kΩ.</p> <p>S2 protocol output impedance of 10 ±3 kΩ is realized by attaching external resistance of 4.7 kΩ.</p> <table border="1"> <thead> <tr> <th>DC_OUT (bus)</th> <th>Output DC</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>4.5 V</td> </tr> <tr> <td>1</td> <td>0 V</td> </tr> <tr> <td>2</td> <td>1.9 V</td> </tr> <tr> <td>3</td> <td>4.5 V</td> </tr> </tbody> </table> | DC_OUT (bus) | Output DC | 0 | 4.5 V | 1 | 0 V | 2 | 1.9 V | 3 | 4.5 V |
| DC_OUT (bus) | Output DC | | | | | | | | | | | | | |
| 0 | 4.5 V | | | | | | | | | | | | | |
| 1 | 0 V | | | | | | | | | | | | | |
| 2 | 1.9 V | | | | | | | | | | | | | |
| 3 | 4.5 V | | | | | | | | | | | | | |
| 55 46 | TRAP1 TRAP2 | 3.8 V | | Connects trap circuit for subcarrier. | | | | | | | | | | |
| 48 | MUTE | — | | <p>Audio signal output mute.</p> <p>Mute OFF at 1.5 V or less</p> <p>Mute ON at 2.5 V or more</p> <p>Mute OFF when open.</p> | | | | | | | | | | |
| 50 | BIAS | 4.5 V | | <p>Internal reference bias ($V_{cc}/2$).</p> <p>Connect to GND via a capacitor.</p> | | | | | | | | | | |

Electrical Characteristics

(Ta=25 °C Vcc=9 V)

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---------------------|--------|--------------------|------|------|------|------|
| Current consumption | Icc | No signal, no load | 40 | 55 | 72 | mA |

Video system (Measurement circuit ; Fig. 1)

| | | | | | | |
|--|-------|---|-----|-----|-----|------|
| Gain | GVv | f=100 kHz, 0.3 Vp-p input | 5.9 | 6.4 | 6.9 | dB |
| Frequency response characteristics | FBWv1 | f=100 kHz, input frequency where output amplitude is -3 dB with 0.3 Vp-p output | 15 | 20 | | MHz |
| Frequency response characteristics (Y/C mix) | FBWv2 | serving as 0 dB | 10 | 15 | — | MHz |
| Input dynamic range | Ddv | f=100 kHz, maximum with distortion < 1.0 % | 1.4 | — | — | Vp-p |
| Cross talk | Vctv | f=4.43 MHz, 1 Vp-p input | — | — | -50 | dB |

Audio system (Measurement circuits ; Fig. 2 to Fig. 5)

| | | | | | | |
|------------------------------------|------------------|---|-----|------|------|-------|
| Gain | GV _A | f=1 kHz, 1 Vp-p input, 5.7 kΩ resistor inserted to input | -1 | 0 | 1 | dB |
| Frequency response characteristics | FBW _A | f=1 kHz, input frequency where output amplitude is -3 dB with 1 Vp-p output serving as 0 dB | 50 | — | — | kHz |
| Total harmonic distortion | THD | f=1 kHz, 2.2 Vp-p input, where 400 Hz HPF+80 kHz LPF are inserted | — | 0.03 | 0.05 | % |
| Input dynamic range | Dd _A | f=1 kHz, maximum with distortion < 0.3 % | 2.8 | 3.0 | — | Vrms |
| Cross talk | Vct _A | f=1 kHz, 1 Vp-p input | — | -90 | -80 | dB |
| Ripple rejection ratio | Vct _A | f=100 Hz, 0.3 Vp-p applied to Vcc | — | -55 | -40 | dB |
| Output DC offset | Voff | Offset voltage between input and output | -30 | — | 30 | mV |
| Residual noise | VN _A | When 400 Hz HPF+30 kHz LPF are inserted | 0 | 20 | 30 | μVrms |
| S/N ratio | S/N | f=1 kHz, 1 Vrms input f _{CL} =400 Hz, f _{CH} =30kHz | | -100 | -90 | dB |

Logic system

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|--|--------------|--------------------------------|------|------|------|---------|
| High level input voltage | V_{IH} | | 3.0 | — | 5.0 | V |
| Low level input voltage | V_{IL} | | 0 | — | 1.5 | V |
| Low level output voltage | V_{OL} | With SDA 3 mA current supplied | 0 | — | 0.4 | V |
| High level input current | I_{IH} | $V_{IH}=4.5V$ | 0 | — | 10 | μA |
| Low level input current | I_{IL} | $V_{IL}=0.4V$ | 0 | — | 10 | μA |
| Maximum clock frequency | f_{SCL} | | 0 | — | 100 | kHz |
| Minimum waiting time for data change | t_{BUF} | | 4.7 | — | — | μs |
| Minimum waiting time for data transfer start | $t_{HD;STA}$ | | 4.0 | — | — | μs |
| Low level clock pulse width | t_{LOW} | | 4.7 | — | — | μs |
| High level clock pulse width | t_{HIGH} | | 4.0 | — | — | μs |
| Minimum waiting time for start preparation | $t_{SU;STA}$ | | 4.7 | — | — | μs |
| Minimum data hold time | $t_{HD;DAT}$ | | 300 | — | — | ns |
| Minimum data preparation time | $t_{SU;DAT}$ | | 250 | — | — | ns |
| Rise time | t_R | | — | — | 1 | μs |
| Fall time | t_F | | — | — | 300 | ns |
| Minimum waiting time for stop preparation | $t_{SU;STO}$ | | 4.7 | — | — | μs |

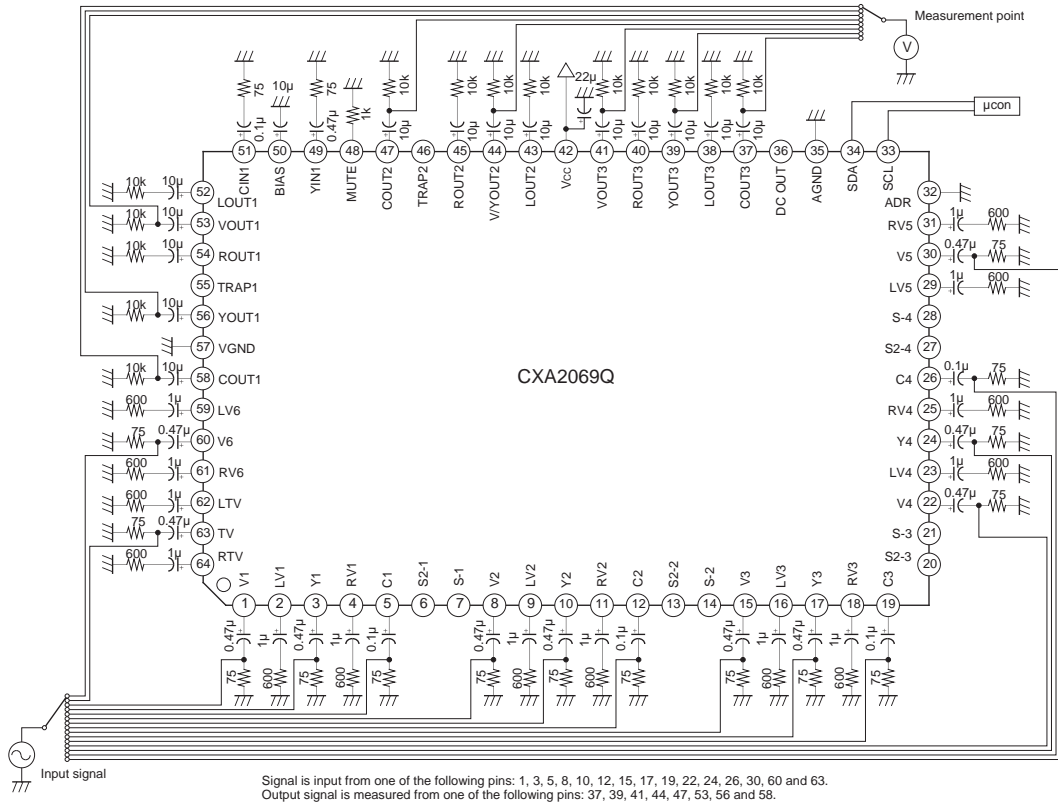


Fig. 1 Video system (gain, frequency response characteristics, input dynamic range, cross talk) measurement circuit

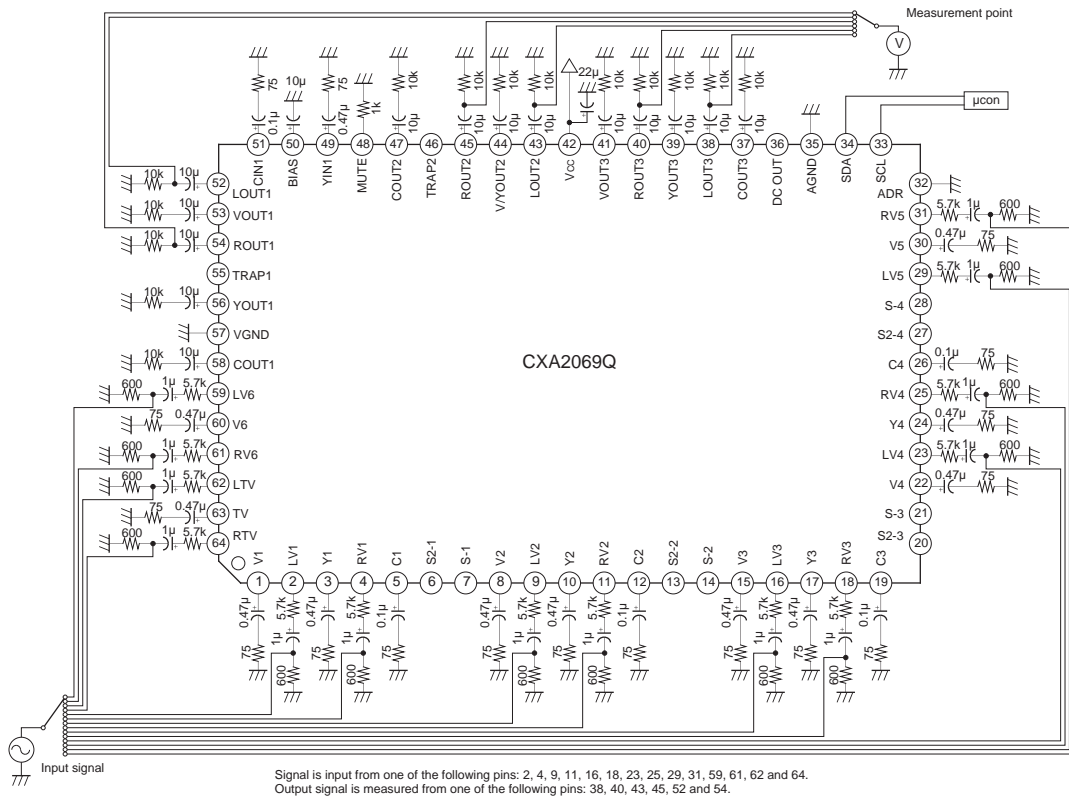


Fig. 2 Audio system (gain, frequency response characteristics, total harmonic distortion, input dynamic range, cross talk) measurement circuit

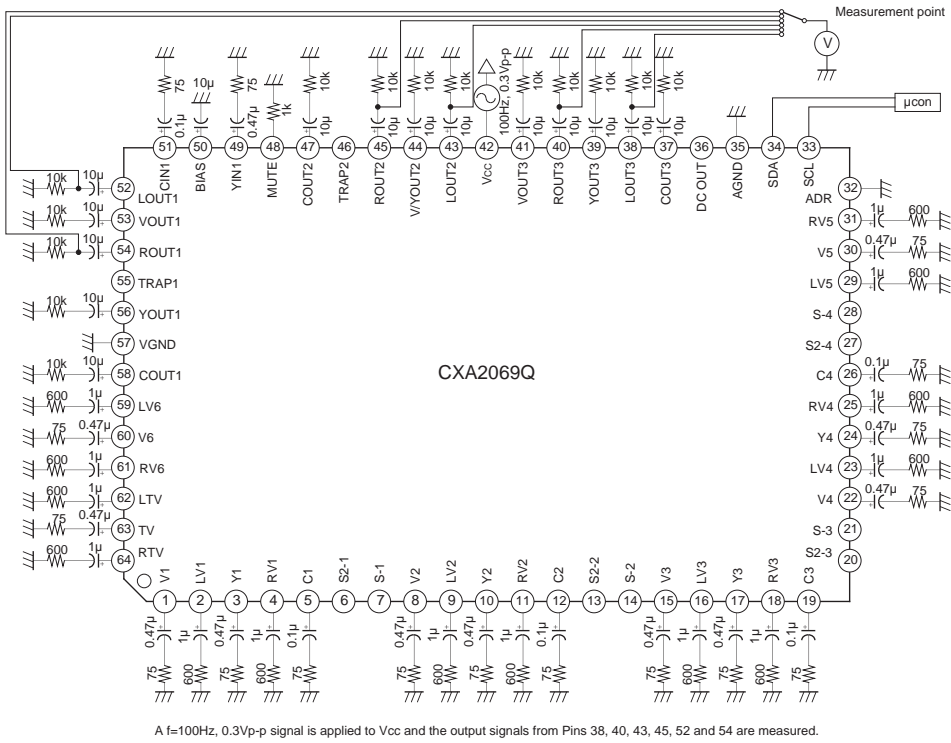


Fig. 3 Audio system (ripple rejection ratio) measurement circuit

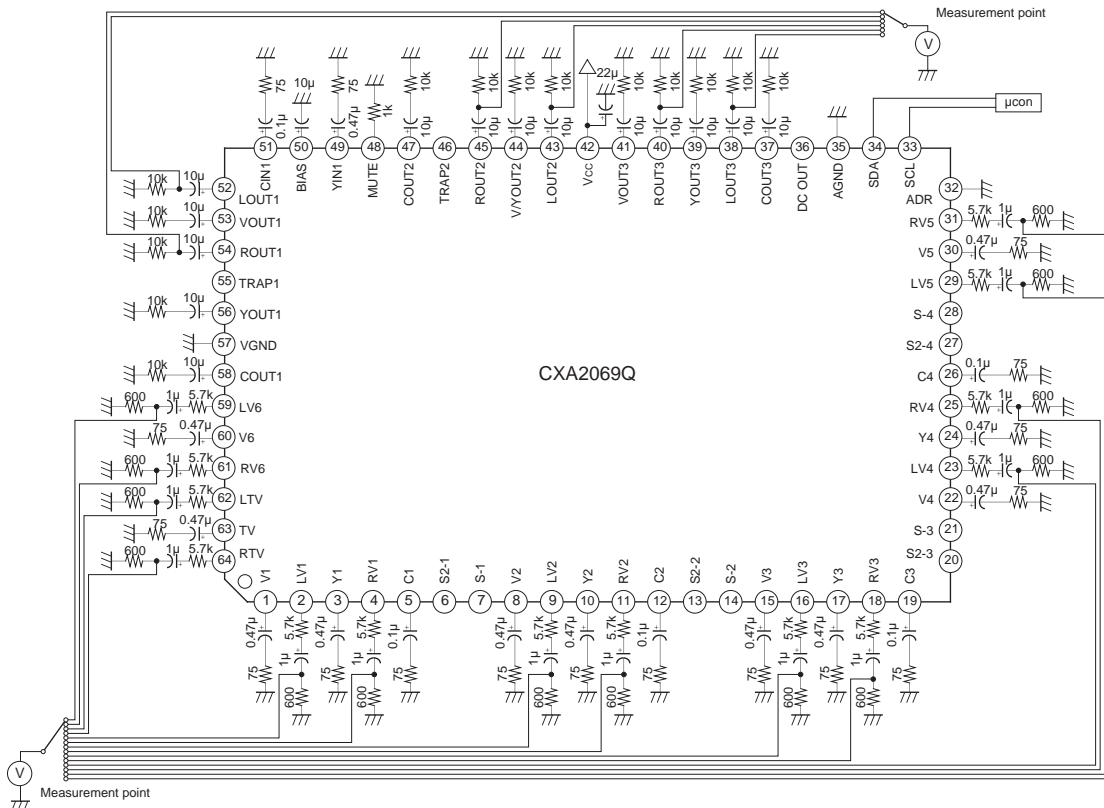


Fig. 4 Audio system (output DC offset voltage) measurement circuit

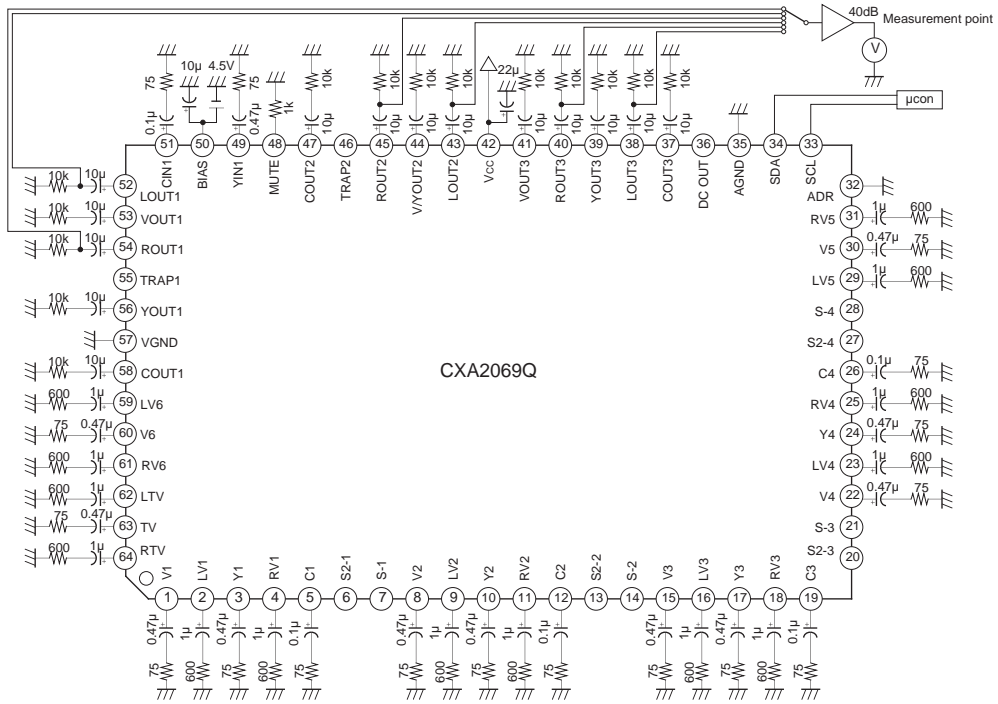
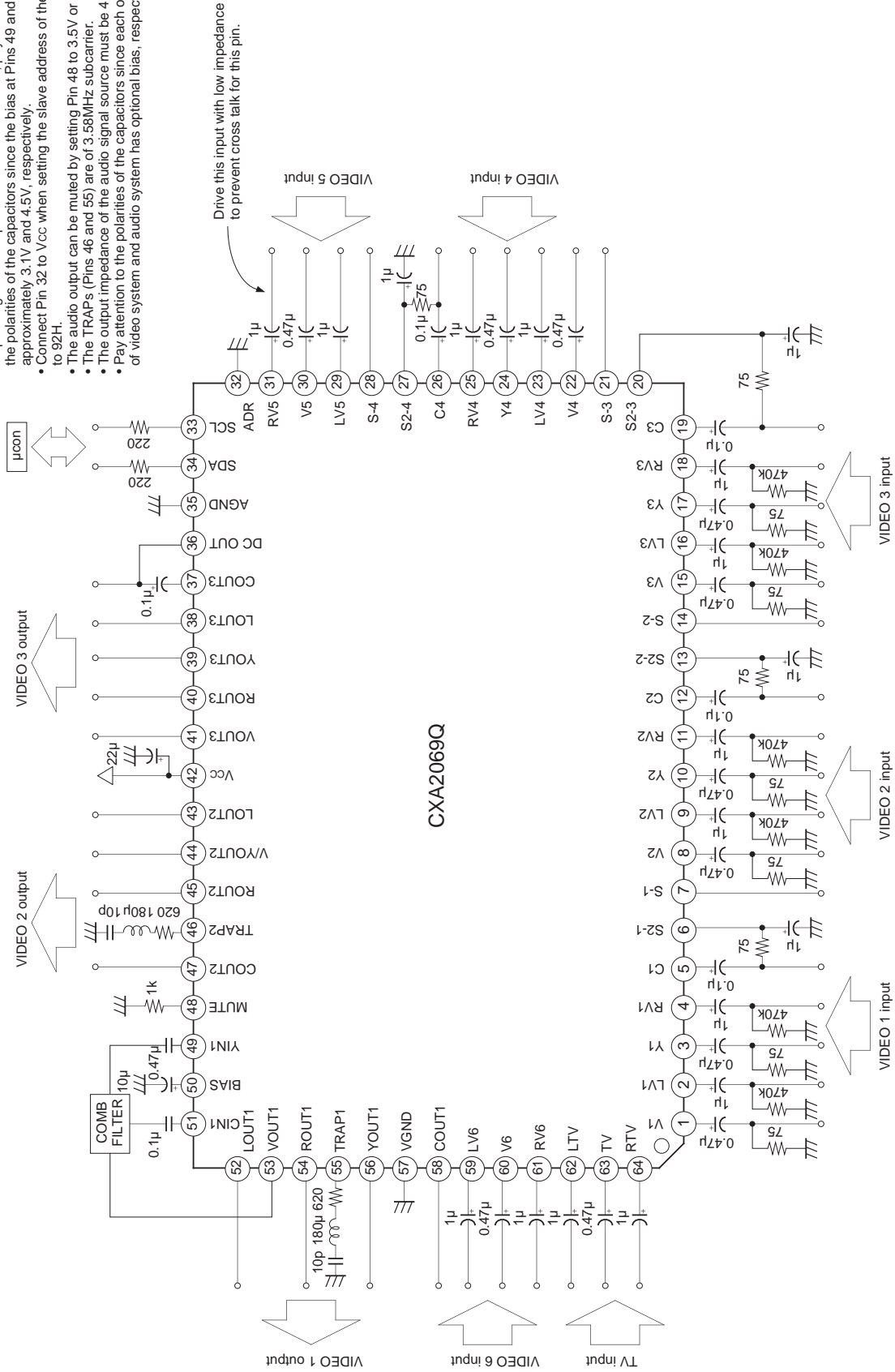


Fig. 5 Audio system (residual noise) measurement circuit

Application Circuit

- Depending on the output bias of the comb filters, pay attention to the polarities of the capacitors since the bias at Pins 49 and 51 is approximately 3.1V and 4.5V, respectively.
- Connect Pin 32 to Vcc when setting the slave address of the IC to 92H.
- The audio output can be muted by setting Pin 48 to 3.5V or more.
- The TRAPs (Pins 46 and 55) are of 3.58MHz subcarrier.
- The output impedance of the audio signal source must be 4.7kΩ.
- Pay attention to the polarities of the capacitors since each output of video system and audio system has optional bias, respectively.



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

I²C BUS Control Signal

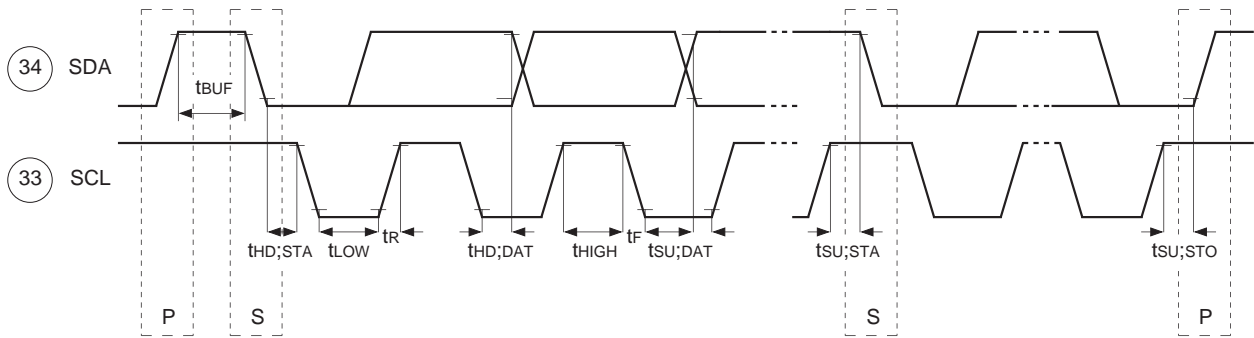


Fig. 6 I²C BUS Control Signal Timing Chart

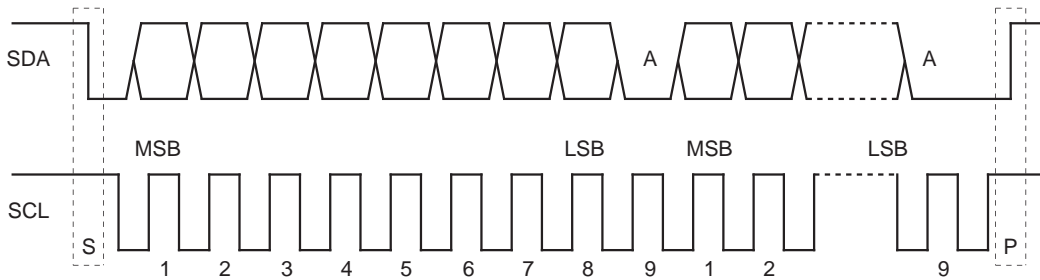
Description of Operation

The CXA2069Q is a TV I²C bus-compatible AV switch IC. The video system and the stereo audio system both have 7 inputs and 3 outputs each. 4 of the 7 video system inputs support S2 and S protocols. The desired inputs can be independently assigned to each output (in the audio system, the left and right channels are processed as one unit) by I²C bus control. However, the same input is assigned to both the video and audio system output 3.

I²C BUS Registers

1) I²C BUS

The I²C bus (inter-IC bus) is an inter-IC bus system developed by Philips. Two lines (SDA—serial data, SCL—serial clock) provide control over start, stop, data transfer, synchronization, and collision avoidance. The IC outputs are either open collector or open drain, forming a bus line in the wired OR format.



- S : Start condition ; SDA is set "Low" when SCL is "High"
- P : Stop condition ; SDA is set "High" when SCL is "High"
- A : Acknowledge ; signal sent from the slave

Data is transmitted by MSB-first. One data unit consists of 8 bits, to which the acknowledge signal, which indicates that the data has been accepted by the slave, is attached at the end. Normally, the slave*1 IC receives data at the rising edge of SCL and the master*2 IC changes data at the falling edge of SCL.

*1 Slave : An IC that is placed under the control of the master.
 In a normal system, all devices excluding the central microcomputer are slaves.
 *2 Master : A central microcomputer or other controlling IC.

2) Control Registers

The CXA2069Q control is exercised by writing 3-byte data into the three 8-bit control registers which control the output selector circuits for the 3 outputs.

| | | | | | | | | | |
|---|---------------|---|-------|---|-------|---|-------|---|---|
| S | Slave address | A | DATA1 | A | DATA2 | A | DATA3 | A | P |
|---|---------------|---|-------|---|-------|---|-------|---|---|

S ; Start condition

A ; Acknowledge

P ; Stop condition

O Control register structure (DATA1 to DATA3)

- All registers are set to "0" during IC power on.
- "*" indicates undefined.

| | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|------------|--------|---------|--------|----|----|--------|-----|-----|
| Slave add. | 1 | 0 | 0 | 1 | 0 | 0 | ADR | R/W |
| DATA1 | A-GAIN | S/COMP1 | V-IN1 | | | A-IN1 | | |
| DATA2 | V/YOUT | S/COMP2 | V-IN2 | | | A-IN2 | | |
| DATA3 | * | S/COMP3 | AV-IN3 | | | DC OUT | | * |

R/W (1) : Read/write mode

0 : Control data write

1 : Status register read

ADR (1) : This bit sets the slave address set by the address pin.

0 : 90H

1 : 92H

A-GAIN (1) : LOOUT1/ROUT1 output gain selector

0 : 0 dB output

1 : -6 dB output

S/COMP1 to S/COMP3 (1 each) : S terminal input/composite signal input selectors

By setting S/COMP1 to "0", when composite signal input is selected, YOUT1/COUT1 output the inputs from YIN1/CIN1 during video 1 output.

0 : Composite signal inputs (TV, V1 to V6 inputs)

1 : S terminal inputs (Y1/C1 to Y4/C4 inputs)

V/YOUT (1) : This bit selects the output to Pin 44 (V/YOUT2).

0 : VOUT (composite signal) output

1 : YOUT (luminance signal) output

V-IN1 to V-IN2 (3 each) : These bits select the input signals output to each video output.

V-IN1 corresponds to the VOUT1 and YOUT1/COUT1 outputs, and V-IN2 to the VOUT2 and YOUT2/COUT2 outputs.

0 : Mute

4 : Selects the V3 and Y3/C3 inputs

1 : Selects the TV input

5 : Selects the V4 and Y4/C4 inputs

2 : Selects the V1 and Y1/C1 inputs

6 : Selects the V5 input

3 : Selects the V2 and Y2/C2 inputs

7 : Selects the V6 input

A-IN1 to A-IN2 (3 each) : These bits select the input signals output to each audio output.

A-IN1 corresponds to the LOUT1/ROUT1 outputs, and A-IN2 to the LOUT2/ROUT2 outputs.

- 0 : Mute
- 1 : Selects the LTV/RTV inputs
- 2 : Selects the LV1/RV1 inputs
- 3 : Selects the LV2/RV2 inputs
- 4 : Selects the LV3/RV3 inputs
- 5 : Selects the LV4/RV4 inputs
- 6 : Selects the LV5/RV5 inputs
- 7 : Selects the LV6/RV6 inputs

AV-IN3 (3) : This bit selects the input signals output to output 3.

Both the video output and the audio output are selected at the same time only for AV-IN3.

- 0 : Mute
- 1 : Selects the TV and LTV/RTV inputs
- 2 : Selects the V1, Y1/C1 and LV1/RV1 inputs
- 3 : Selects the V2, Y2/C2 and LV2/RV2 inputs
- 4 : Selects the V3, Y3/C3 and LV3/RV3 inputs
- 5 : Selects the V4, Y4/C4 and LV4/RV4 inputs
- 6 : Selects the V5 and LV5/RV5 inputs
- 7 : Selects the V6 and LV6/RV6 inputs

DC OUT (2) : These bits set the DC voltage output from Pin 35 (DC OUT).

- 0 : 4.5 V
- 1 : 0 V
- 2 : 1.9 V
- 3 : 4.5 V

3) Status Registers

- When reading two bytes

| | | | | | | | |
|---|---------------|---|-------|---|-------|----|---|
| S | Slave address | A | DATA1 | A | DATA2 | NA | P |
|---|---------------|---|-------|---|-------|----|---|

- When reading one byte

| | | | | | |
|---|---------------|---|-------|----|---|
| S | Slave address | A | DATA1 | NA | P |
|---|---------------|---|-------|----|---|

- S ; Start condition
- A ; Acknowledge
- NA ; No acknowledge
- P ; Stop condition

When communication is to be terminated in the status register reading mode, the “no-acknowledge” signal is needed to assure that the master does not issue the acknowledge signal to the slave.

It is possible to read only DATA1 of the status register by sending the no-acknowledge signal after DATA1.

O Status register structure (DATA1 to DATA2)

| | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|------------|-------|-------|-------|-------|------|----|------|----|
| Slave add. | 1 | 0 | 0 | 1 | 0 | 0 | ADR | 1 |
| DATA1 | S1SEL | S2SEL | S3SEL | S4SEL | S-C1 | | S-C2 | |
| DATA2 | S1SEL | S2SEL | S3SEL | S4SEL | S-C3 | | S-C4 | |

S1SEL to S4SEL (1 each) : S-1 to S-4 pin status
 0 ; S-1 to S-4 pins are not grounded.
 1 ; S-1 to S-4 pins are grounded.
 S1SEL to S4SEL are actually determined by comparing the S-1 to S-4 pin DC voltages with 3.5 V.

| S-1 to S-4 pin DC voltage | S1SEL to S4SEL |
|---------------------------|----------------|
| 3.5 V or more | 0 |
| 3.5 V or less | 1 |

S-C1, S-C2, S-C3, S-C4 (2 each) : S2-1, S2-2, S2-3 and S2-4 pin status

0 ; 4 : 3 video signal
 1 ; 4 : 3 letter-box signal
 2 ; 16 : 9 video squeezed signal
 3 ; No signal

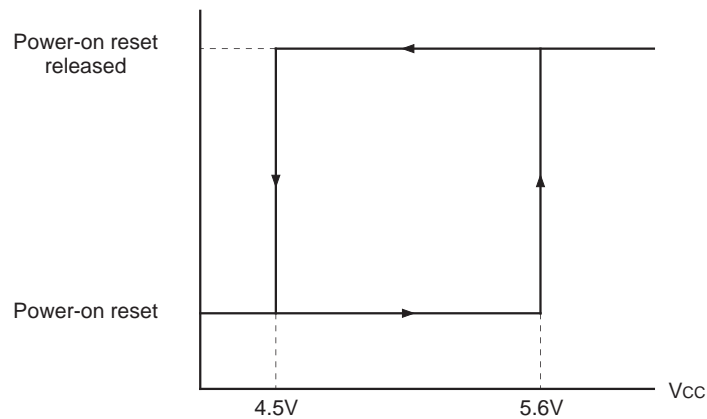
S-C1 to S-C4 are actually determined by comparing the S2-1 to S2-4 pin DC voltages with two threshold. However, when the S-1 to S-4 pins are open, the outputs are fixed to "3".

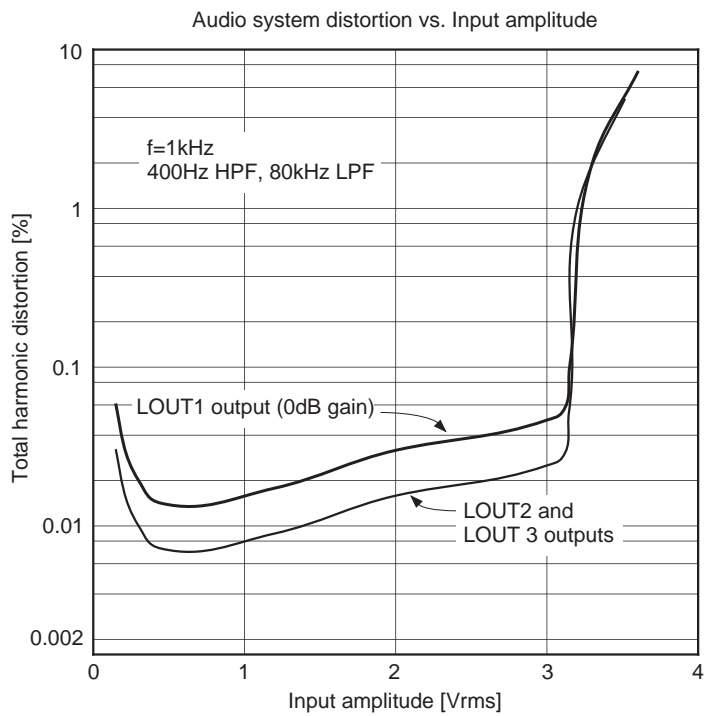
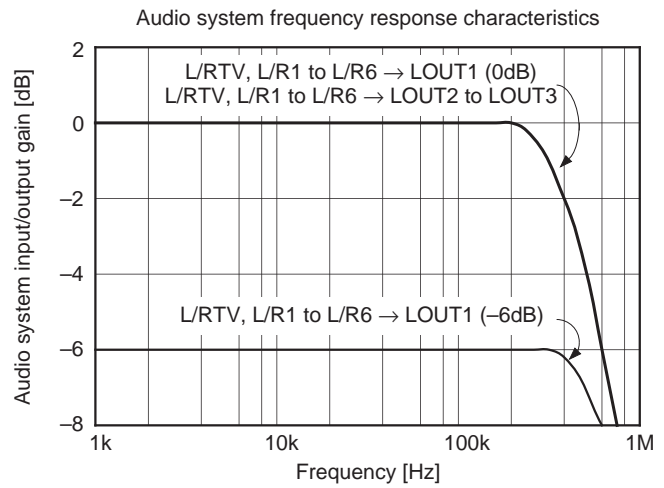
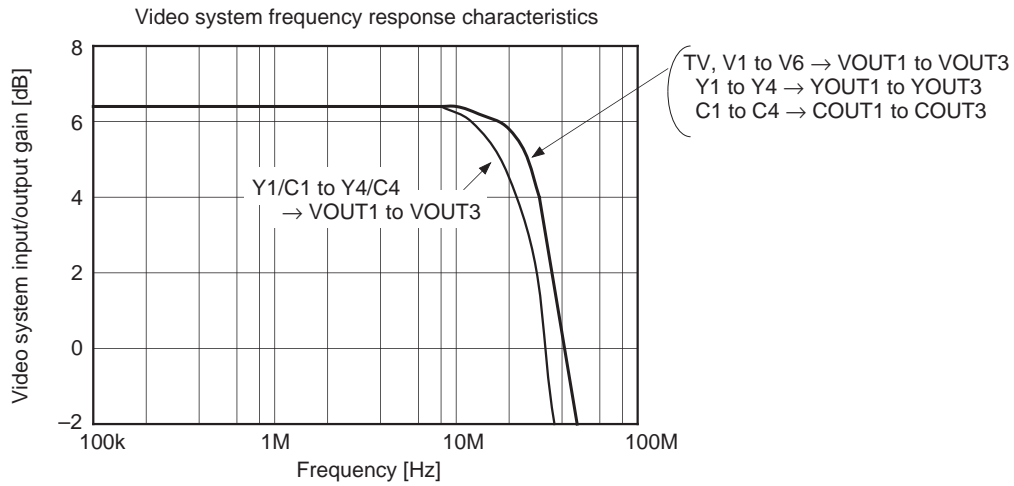
| S2-1 to S2-4 pin DC voltage | S-C1 to S-C4 |
|--------------------------------|--------------|
| 1.3 V or less | 0 |
| 1.3 V or more to 2.5 V or less | 1 |
| 2.5 V or more | 2 |
| S-1 to S-4 OPEN | 3 |

4) Power-on Reset

The CXA2069Q has an internal power-on reset function that sets each control register to "0" during IC power ON.

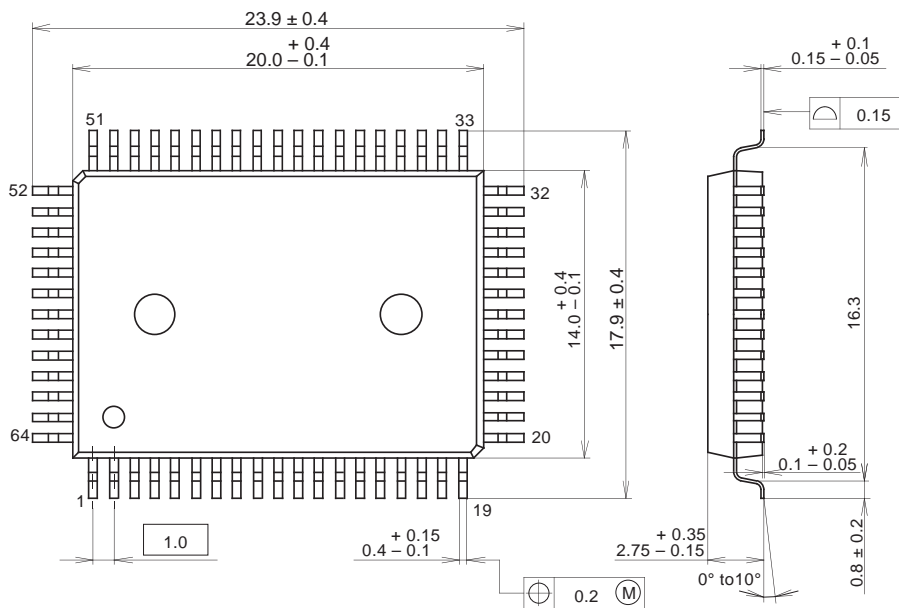
The power-on reset V_{TH} has hysteresis.





Package Outline Unit : mm

64PIN QFP(PLASTIC)



PACKAGE STRUCTURE

| | |
|------------|---------------|
| SONY CODE | QFP-64P-L01 |
| EIAJ CODE | QFP064-P-1420 |
| JEDEC CODE | _____ |

| | |
|------------------|--------------------------|
| PACKAGE MATERIAL | EPOXY RESIN |
| LEAD TREATMENT | SOLDER/PALLADIUM PLATING |
| LEAD MATERIAL | 42/COPPER ALLOY |
| PACKAGE MASS | 1.5g |