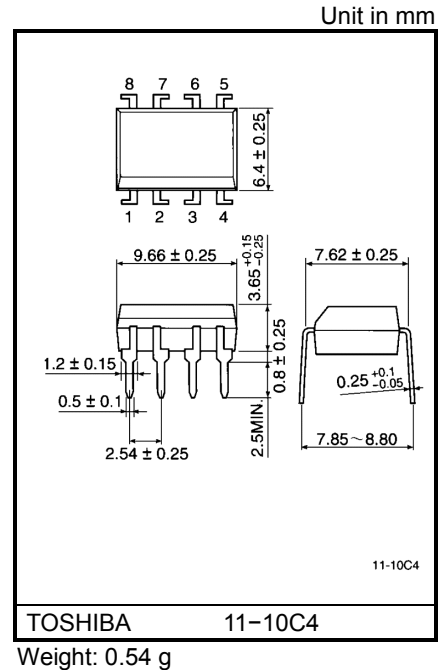


TLP2630

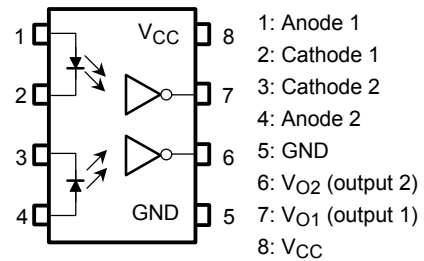
Digital Logic Isolation
 Tele-Communication
 Analog Data Equipment Control
 Microprocessor System Interface

The TOSHIBA TLP2630 dual photocoupler consists of a pair of GaAlAs light emitting diode and integrated high gain, high speed photodetector.
 The output of the detector circuit is an open collector, schottky clamped transistor. This unit is 8-lead DIP.

- Input current threshold: $I_F = 5\text{mA}(\text{max.})$
- LSTTL/TTL compatible: 5V supply
- Switching speed: 10MBd(typ.)
- Guaranteed performance over temperature: 0~70°C
- Isolation voltage: 2500V_{rms}(min.)
- UL recognized: UL1577, file no. E67349



Pin Configuration (top view)

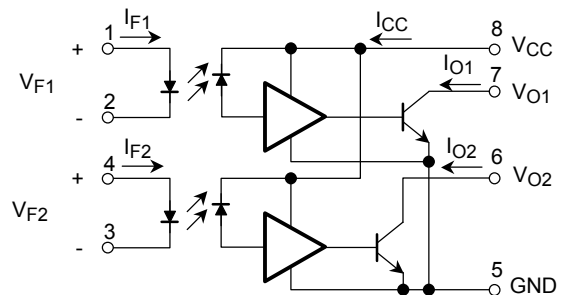


Truth Table (positive logic)

Input	Output
H	L
L	H

A 0.01 to 0.1μF bypass capacitor must be connected between pins 8 and 5 (see Note 1).

Schematic



Maximum Ratings (no derating required up to 70°C)

Characteristic		Symbol	Rating	Unit
LED	Forward current(each channel)	I_F	20	mA
	Pulse forward current (each channel)*	I_{FP}	30	mA
	Reverse voltage(each channel)	V_R	5	V
Detector	Output current(each channel)	I_O	16	mA
	Output voltage(each channel)	V_O	-0.5~7	V
	Supply voltage (1 minute maximum)	V_{CC}	7	V
	Output collector power dissipation(each channel)	P_O	40	mW
Operating temperature range		T_{stg}	-55~125	°C
Storage temperature range		T_{opr}	-40~85	°C
Lead soldering temperature (10 s) (Note 1)		T_{sol}	260	°C
Isolation voltage (AC, 1 min., R.H.≤ 60%, Note 3)		BV_S	2500	Vrms

* $t \leq 1$ msec duration.

Recommended Operating Conditions

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Input current, low level, each channel	I_{FL}	0	—	250	μA
Input current, high level, each channel	I_{FH}	6.3*	—	15	mA
Supply voltage, output	V_{CC}	4.5	5	5.5	V
Fan out(TTL load, each channel)	N	—	—	8	
Operating temperature	T_{opr}	0	—	70	°C

* 6.3mA is a guard banded value which allows for at least 20% CTR degradation.
Initial input current threshold value is 5.0mA or less.

Electrical Characteristics (Ta = 0~70°C, unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.*	Max.	Unit
Input forward voltage (each channel)	V_F	$I_F = 10\text{mA}$, $T_a = 25^\circ\text{C}$	—	1.65	1.75	V
Input diode temperature coefficient(each channel)	$\Delta V_F / \Delta T_a$	$I_F = 10\text{mA}$	—	-2.0	—	mV / °C
Input reverse breakdown voltage(each channel)	BV_R	$I_R = 10\mu\text{A}$, $T_a = 25^\circ\text{C}$	5	—	—	V
Input capacitance (each channel)	C_T	$V_F = 0$, $f = 1\text{MHz}$	—	45	—	pF
High level output current (each channel)	I_{OH}	$V_{CC} = 5.5\text{V}$, $V_O = 5.5\text{V}$ $I_F = 250\mu\text{A}$	—	1	250	μA
Low level output voltage (each channel)	V_{OL}	$V_{CC} = 5.5\text{V}$, $I_F = 5\text{mA}$ $I_{OL}(\text{sinking}) = 13\text{mA}$	—	0.4	0.6	V
High level supply current (both channels)	I_{CCH}	$V_{CC} = 5.5\text{V}$, $I_F = 0$	—	14	30	mA
Low level supply current (both channels)	I_{CCL}	$V_{CC} = 5.5\text{V}$, $I_F = 10\text{mA}$	—	24	36	mA
Isolation voltage	R_S	$V_S = 500\text{V}$, R.H. $\leq 60\%$ (Note 3)	—	10^{14}	—	Ω
Capacitance(input-output)	C_S	$f = 1\text{MHz}$ (Note 3)	—	0.6	—	pF
Input-input leakage current	I_{I-I}	R.H. $\leq 60\%$, $t = 5\text{s}$ $V_{I-I} = 500\text{V}$ (Note 6)	—	0.005	—	μA
Resistance(input-input)	R_{I-I}	$V_{I-I} = 500\text{V}$ (Note 6)	—	10^{11}	—	Ω
Capacitance(input-input)	C_{I-I}	$f = 1\text{MHz}$ (Note 6)	—	0.25	—	pF

* All typical values are at $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$.

Switching Characteristics (Ta =25°C , VCC=5V)

Characteristic	Symbol	Test Circuit	Test Condition	Min.	Typ.	Max.	Unit
Propagation delay time to low output level	t_{pHL}	1	$I_F = 0 \rightarrow 7.5\text{mA}$, $R_L = 350\Omega$ $C_L = 15\text{pF}$ (each channel)	—	60	75	ns
Propagation delay time to high output level	t_{pLH}	1	$I_F = 7.5\text{mA} \rightarrow 0$, $R_L = 350\Omega$ $C_L = 15\text{pF}$ (each channel)	—	60	75	ns
Output rise a time,output fall time(10~90%)	t_r, t_f	1	$I_F = 0 \rightleftharpoons 7.5\text{mA}$, $R_L = 350\Omega$ $C_L = 15\text{pF}$ (each channel)	—	30	—	ns
Common mode transient immunity at high output level	CM_H	2	$I_F = 0$, $R_L = 350\Omega$ $V_{CM} = 200\text{V}$ $V_{O(\text{min.})} = 2\text{V}$ (each channel, Note 4)	—	200	—	V / μs
Common mode transient immunity at low output level	CM_L	2	$I_F = 7.5\text{mA}$, $R_L = 350\Omega$ $V_{CM} = 200\text{V}$ $V_{O(\text{max.})} = 0.8\text{V}$ (each channel, Note 5)	—	-500	—	V / μs

(Note 1) 2mm below seating plane.

(Note 2) The V_{CC} supply voltage to each TLP2630 isolator must be bypassed by a 0.01 μF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins each device.

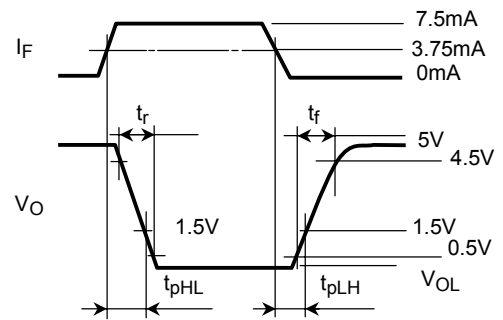
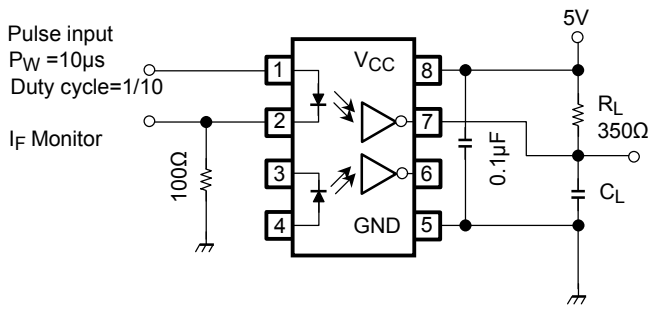
(Note 3) Device considered a two-terminal device: Pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.

(Note 4) CM_H ·the maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the high state(i.e., $V_{OUT} > 2.0\text{V}$)

(Note 5) CM_L ·the maximum tolerable rate of fall of the common mode voltage to ensure the output will remain in the low output state(i.e., $V_{OUT} > 0.8\text{V}$)
Measured in volts per microsecond(V / μs).

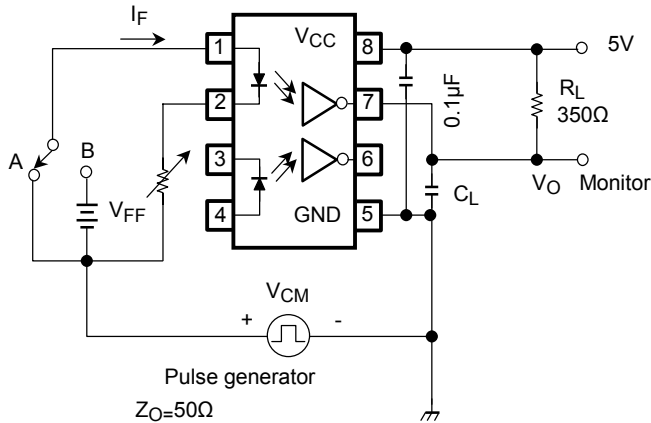
(Note 6) Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

Test Circuit 1. t_{pHL} And t_{pLH}

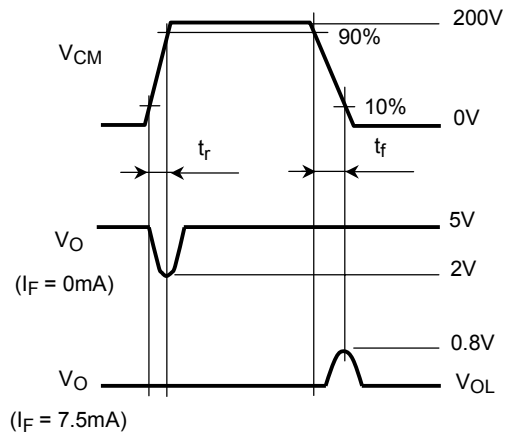


* C_L is approximately 15pF which includes probe and stray wiring capacitance.

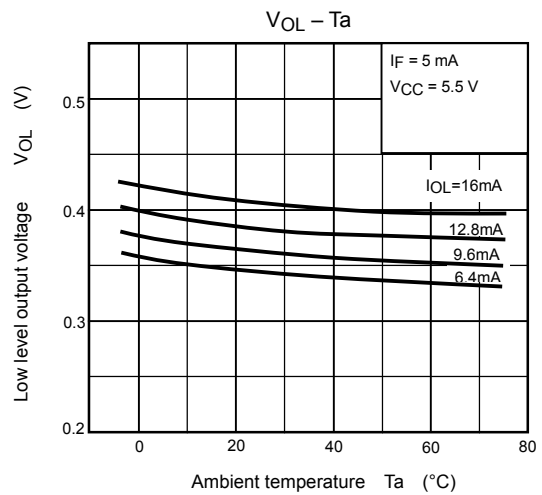
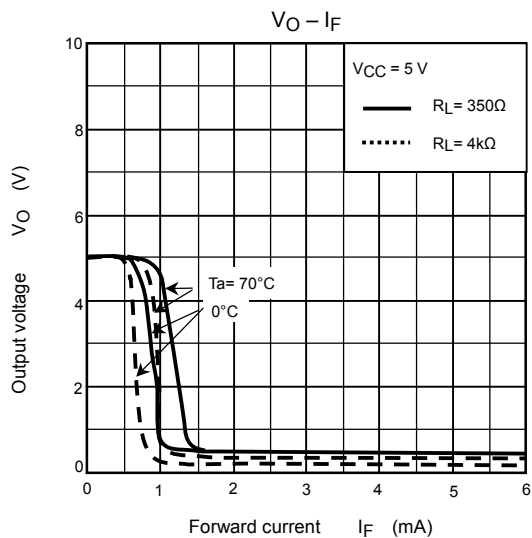
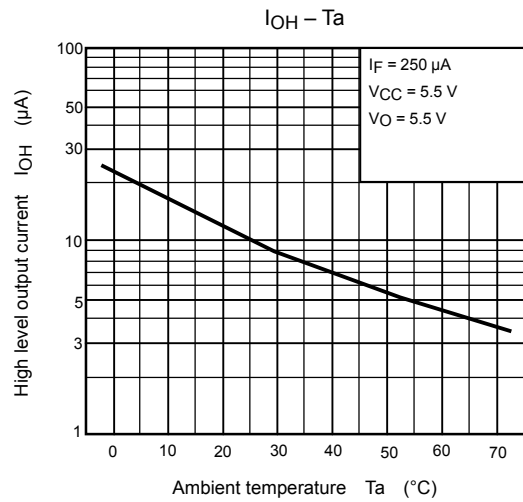
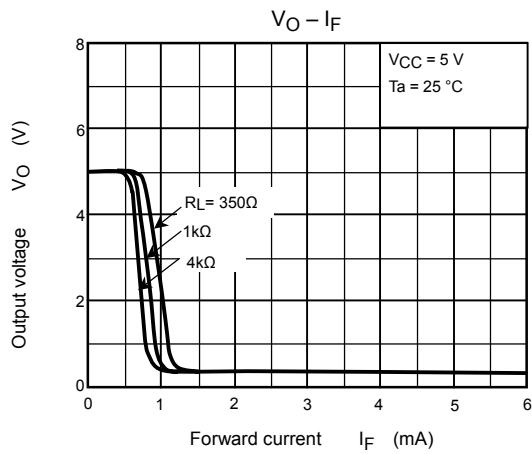
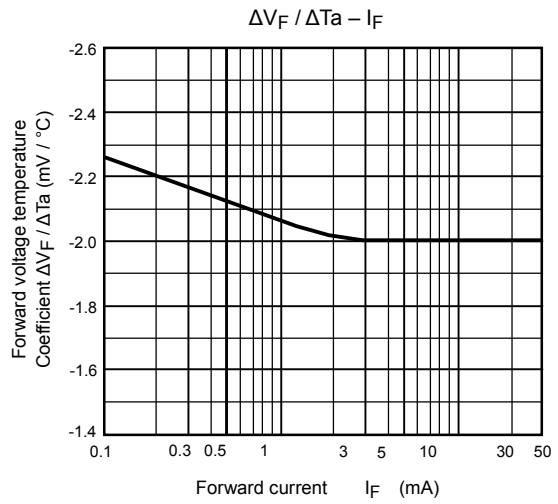
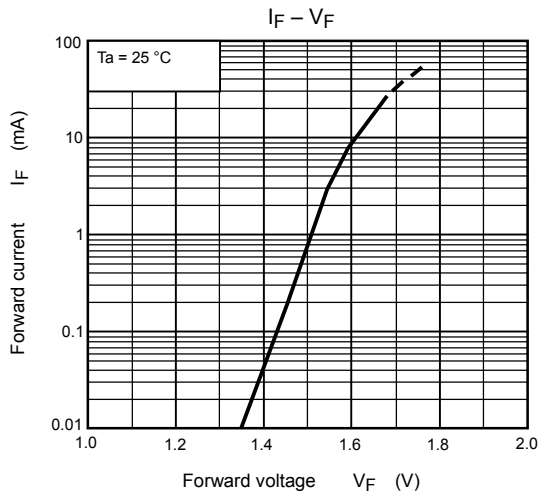
Test Circuit 2. Transient Immunity And Typical Waveforms.

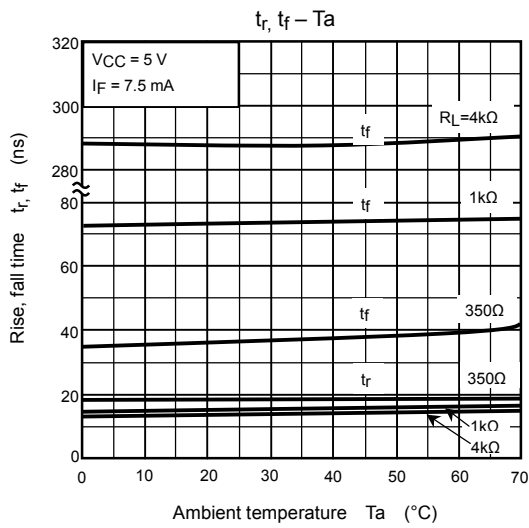
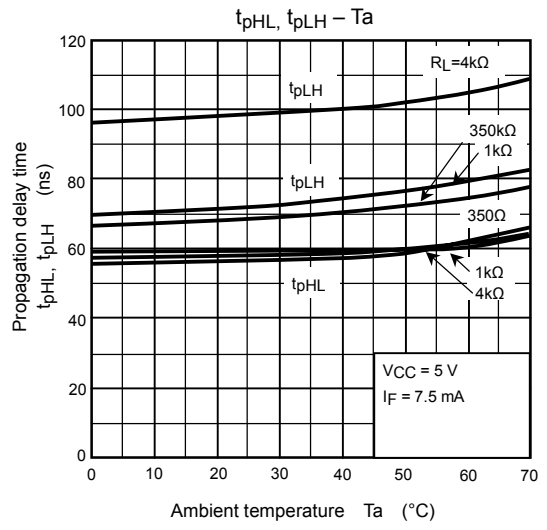
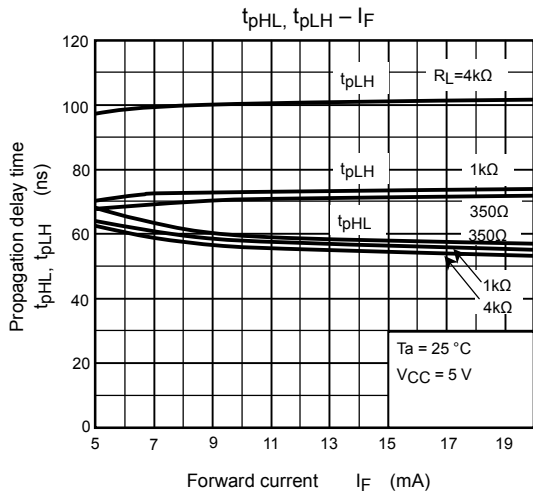


$$CM_H = \frac{160(V)}{t_r(\mu s)}, CM_L = \frac{160(V)}{t_f(\mu s)}$$



* C_L is approximately 15pF which includes probe and stray wiring capacitance.





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