National
Semiconductor

June 2006

LMC660
CMOS Quad Operational Amplifier

General Description

The LMC660 CMOS Quad operational amplifier is ideal for operation from a single supply. It operates from +5V to +15.5V and features rail-to-rail output swing in addition to an input common-mode range that includes ground. Performance limitations that have plagued CMOS amplifiers in the past are not a problem with this design. Input V_{OS}, drift, and broadband noise as well as voltage gain into realistic loads (2 kΩ and 600Ω) are all equal to or better than widely accepted bipolar equivalents.

This chip is built with National's advanced Double-Poly Silicon-Gate CMOS process.

See the LMC662 datasheet for a dual CMOS operational amplifier with these same features.

Features

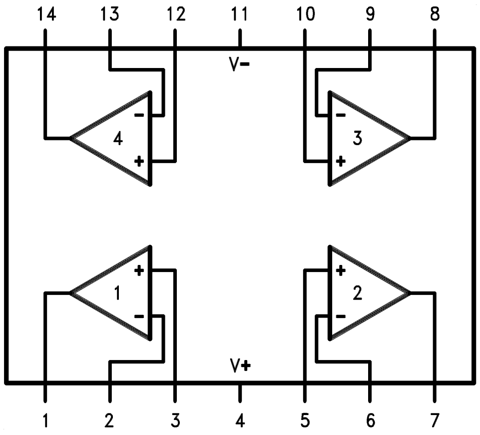
- Rail-to-rail output swing
- Specified for 2 kΩ and 600Ω loads
- High voltage gain: 126 dB
- Low input offset voltage: 3 mV
- Low offset voltage drift: 1.3 μV/˚C
- Ultra low input bias current: 2 fA
- Input common-mode range includes V^-
- Operating range from +5V to +15.5V supply
- I_{SS} = 375 μA/amplifier; independent of V^+
- Low distortion: 0.01% at 10 kHz
- Slew rate: 1.1 V/μs

Applications

- High-impedance buffer or preamplifier
- Precision current-to-voltage converter
- Long-term integrator
- Sample-and-Hold circuit
- Peak detector
- Medical instrumentation
- Industrial controls
- Automotive sensors

Connection Diagram

14-Pin SOIC/MDIP



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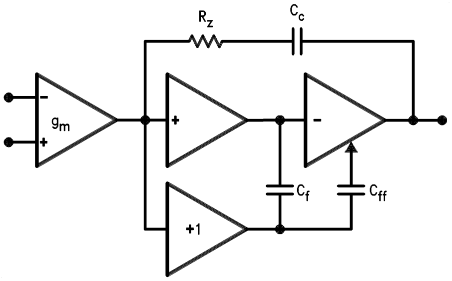
LMC660 Circuit Topology (Each Amplifier)



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Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Differential Input Voltage	±Supply Voltage
Supply Voltage	16V
Output Short Circuit to V^+	(Note 11)
Output Short Circuit to V^-	(Note 1)
Lead Temperature	
(Soldering, 10 sec.)	260˚C
Storage Temp. Range	−65˚C to +150˚C
Voltage at Input/Output Pins	$(V^+) + 0.3V, (V^-) - 0.3V$
Current at Output Pin	±18 mA
Current at Input Pin	±5 mA
Current at Power Supply Pin	35 mA
Power Dissipation	(Note 2)
Junction Temperature	150˚C
ESD tolerance (Note 8)	1000V

Operating Ratings

Temperature Range	
LMC660AI	$-40˚C \le T_J \le +85˚C$
LMC660C	$0˚C \le T_J \le +70˚C$
Supply Voltage Range	4.75V to 15.5V
Power Dissipation	(Note 9)
Thermal Resistance (θ_{JA}) (Note 10)	
14-Pin SOIC	115˚C/W
14-Pin MDIP	85˚C/W

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for $T_J = 25˚C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M\Omega$ unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC660AI	LMC660C	Units
			Limit (Note 4)	Limit (Note 4)	
Input Offset Voltage		1	3 **3.3**	6 **6.3**	mV max
Input Offset Voltage Average Drift		1.3			μV/˚C
Input Bias Current		0.002	**4**	**2**	pA max
Input Offset Current		0.001	**2**	**1**	pA max
Input Resistance		>1			TeraΩ
Common Mode Rejection Ratio	$0V \le V_{CM} \le 12.0V$ $V^+ = 15V$	83	70 **68**	63 **62**	dB min
Positive Power Supply Rejection Ratio	$5V \le V^+ \le 15V$ $V_O = 2.5V$	83	70 **68**	63 **62**	dB min
Negative Power Supply Rejection Ratio	$0V \le V^- \le -10V$	94	84 **83**	74 **73**	dB min
Input Common-Mode Voltage Range	$V^+ = 5V$ & $15V$ For CMRR ≥ 50 dB	−0.4	−0.1 **0**	−0.1 **0**	V max
		$V^+ - 1.9$	$V^+ - 2.3$ $\mathbf{V^+ - 2.5}$	$V^+ - 2.3$ $\mathbf{V^+ - 2.4}$	V min
Large Signal Voltage Gain	$R_L = 2\ k\Omega$ (Note 5) Sourcing	2000	440 **400**	300 **200**	V/mV min
	Sinking	500	180 **120**	90 **80**	V/mV min
	$R_L = 600\Omega$ (Note 5) Sourcing	1000	220 **200**	150 **100**	V/mV min
	Sinking	250	100 **60**	50 **40**	V/mV min

DC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1MΩ unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC660AI	LMC660C	Units
			Limit (Note 4)	**Limit** (Note 4)	
Output Swing	V^+ = 5V R_L = 2 kΩ to $V^+/2$	4.87	4.82 **4.79**	4.78 **4.76**	V min
		0.10	0.15 **0.17**	0.19 **0.21**	V max
	V^+ = 5V R_L = 600Ω to $V^+/2$	4.61	4.41 **4.31**	4.27 **4.21**	V min
		0.30	0.50 **0.56**	0.63 **0.69**	V max
	V^+ = 15V R_L = 2 kΩ to $V^+/2$	14.63	14.50 **14.44**	14.37 **14.32**	V min
		0.26	0.35 **0.40**	0.44 **0.48**	V max
	V^+ = 15V R_L = 600Ω to $V^+/2$	13.90	13.35 **13.15**	12.92 **12.76**	V min
		0.79	1.16 **1.32**	1.45 **1.58**	V max
Output Current V^+ = 5V	Sourcing, V_O = 0V	22	16 **14**	13 **11**	mA min
	Sinking, V_O = 5V	21	16 **14**	13 **11**	mA min
Output Current V^+ = 15V	Sourcing, V_O = 0V	40	28 **25**	23 **21**	mA min
	Sinking, V_O = 13V (Note 11)	39	28 **24**	23 **20**	mA min
Supply Current	All Four Amplifiers V_O = 1.5V	1.5	2.2 **2.6**	2.7 **2.9**	mA max

AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25˚C. **Boldface** limits apply at the temperature extremes. V^+ = 5V, V^- = 0V, V_{CM} = 1.5V, V_O = 2.5V and R_L > 1MΩ unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC660AI	LMC660C	Units
			Limit (Note 4)	**Limit** (Note 4)	
Slew Rate	(Note 6)	1.1	0.8 **0.6**	0.8 **0.7**	V/µs min
Gain-Bandwidth Product		1.4			MHz
Phase Margin		50			Deg
Gain Margin		17			dB
Amp-to-Amp Isolation	(Note 7)	130			dB
Input Referred Voltage Noise	F = 1 kHz	22			$nV/\sqrt{Hz}$
Input Referred Current Noise	f = 1 kHz	0.0002			$pA/\sqrt{Hz}$

AC Electrical Characteristics (Continued)

Unless otherwise specified, all limits guaranteed for $T_J = 25^\circ C$. **Boldface** limits apply at the temperature extremes. $V^+ = 5V$, $V^- = 0V$, $V_{CM} = 1.5V$, $V_O = 2.5V$ and $R_L > 1M\Omega$ unless otherwise specified.

Parameter	Conditions	Typ (Note 4)	LMC660AI	LMC660C	Units
			Limit (Note 4)	Limit (Note 4)	
Total Harmonic Distortion	f = 10 kHz, $A_V = -10$ $R_L = 2\ k\Omega$, $V_O = 8\ V_{PP}$ $V^+ = 15V$	0.01			%

Note 1: Applies to both single supply and split supply operation. Continuous short circuit operation at elevated ambient temperature and/or multiple Op Amp shorts can result in exceeding the maximum allowed junction temperature of 150˚C. Output currents in excess of ±30 mA over long term may adversely affect reliability.

Note 2: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/\theta_{JA}$.

Note 3: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Note 4: Typical values represent the most likely parametric norm. Limits are guaranteed by testing or correlation.

Note 5: $V^+ = 15V$, $V_{CM} = 7.5V$ and R_L connected to 7.5V. For Sourcing tests, $7.5V \le V_O \le 11.5V$. For Sinking tests, $2.5V \le V_O \le 7.5V$.

Note 6: $V^+ = 15V$. Connected as Voltage Follower with 10V step input. Number specified is the slower of the positive and negative slew rates.

Note 7: Input referred. $V^+ = 15V$ and $R_L = 10\ k\Omega$ connected to $V^+/2$. Each amp excited in turn with 1 kHz to produce $V_O = 13\ V_{PP}$.

Note 8: Human Body Model is 1.5 kΩ in series with 100 pF.

Note 9: For operating at elevated temperatures the device must be derated based on the thermal resistance θ_{JA} with $P_D = (T_J - T_A)/\theta_{JA}$.

Note 10: All numbers apply for packages soldered directly into a PC board.

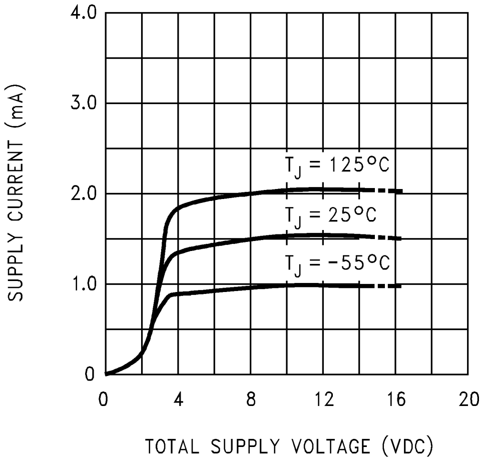
Note 11: Do not connect output to V^+ when V^+ is greater than 13V or reliability may be adversely affected.

Ordering Information

Package	Temperature Range		Transport Media	NSC Drawing
	Industrial −40˚C to +85˚C	Commercial 0˚C to +70˚C		
14-Pin SOIC	LMC660AIM	LMC660CM	Rail	M14A
	LMC660AIMX	LMC660CMX	Tape and Reel	
14-Pin M DIP	LMC660AIN	LMC660CN	Rail	N14A

Typical Performance Characteristics $V_S = \pm 7.5V$, $T_A = 25^{\circ}C$ unless otherwise specified.

Supply Current vs. Supply Voltage



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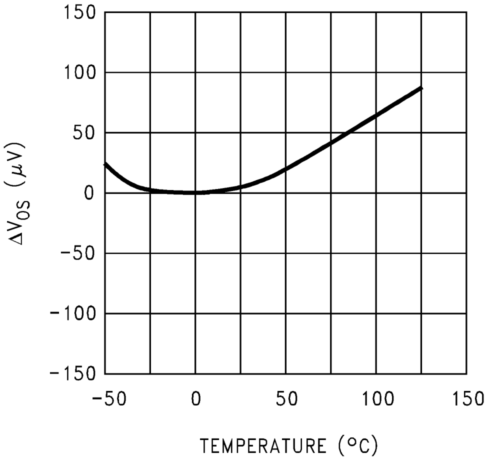
Offset Voltage



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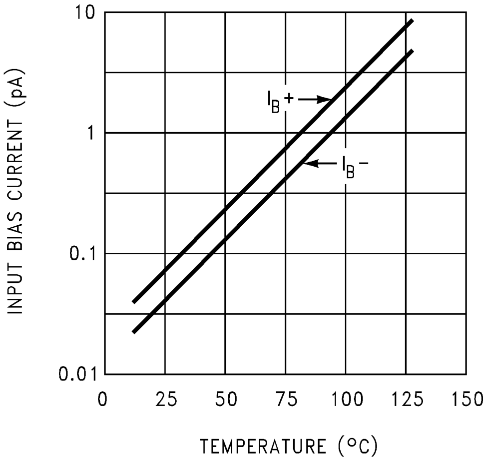
Input Bias Current



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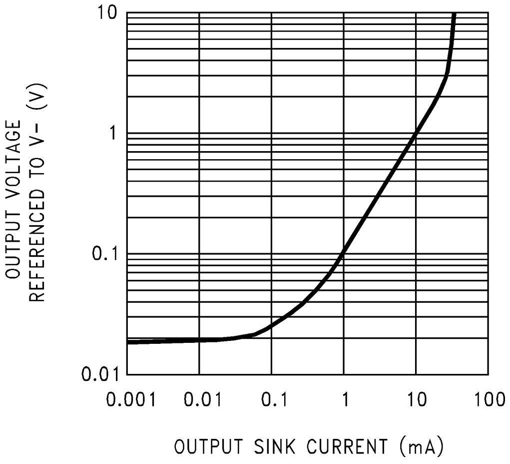
Output Characteristics Current Sinking



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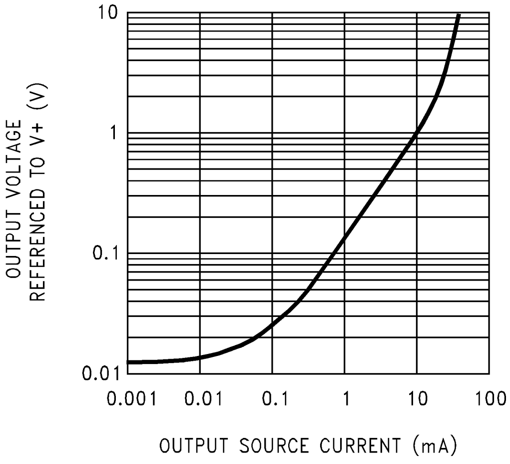
Output Characteristics Current Sourcing



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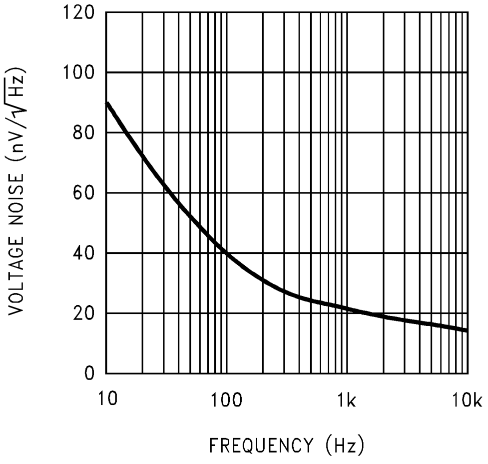
Input Voltage Noise vs. Frequency



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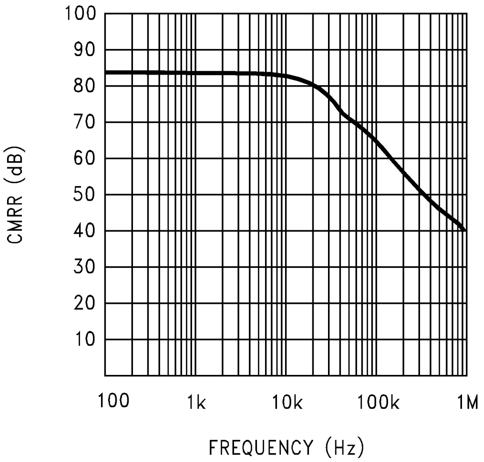
Typical Performance Characteristics V_S = ±7.5V, T_A = 25˚C unless otherwise specified. (Continued)

CMRR vs. Frequency



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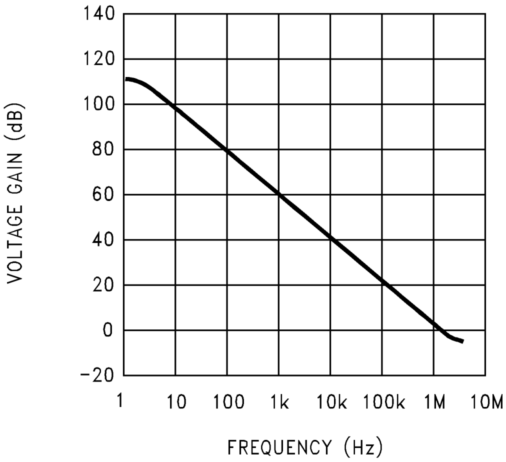
Open-Loop Frequency Response



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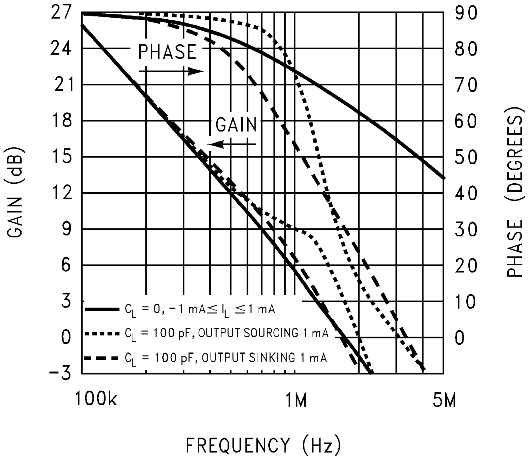
Frequency Response vs. Capacitive Load



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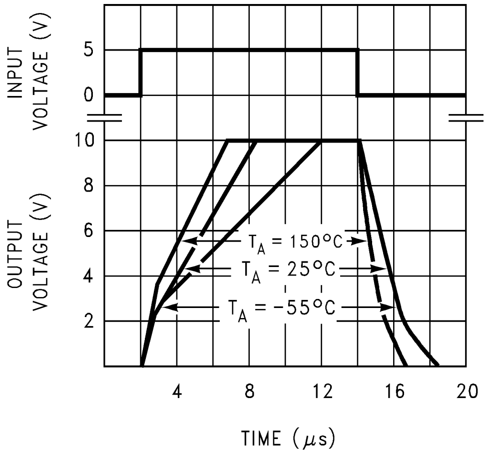
Non-Inverting Large Signal Pulse Response



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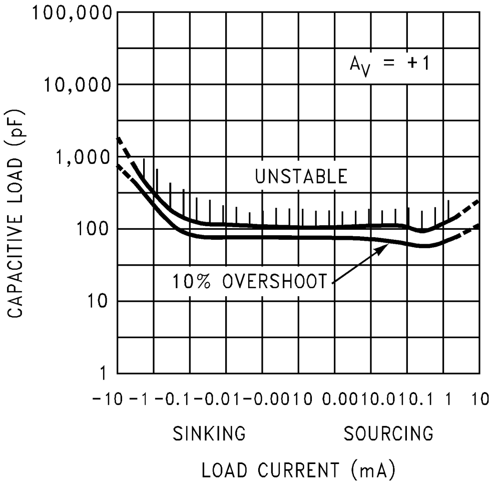
Stability vs. Capacitive Load



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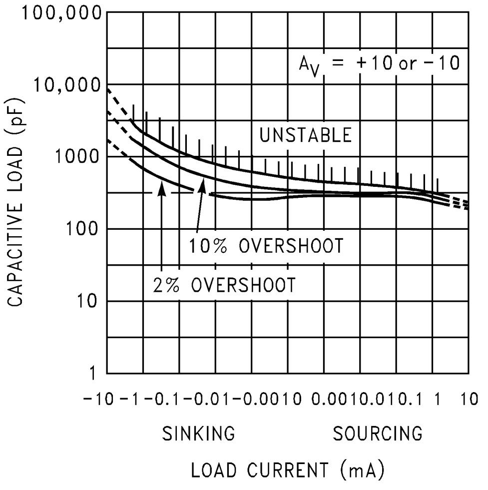
Stability vs. Capacitive Load



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Application Hints

AMPLIFIER TOPOLOGY

The topology chosen for the LMC660, shown in *Figure 1*, is unconventional (compared to general-purpose op amps) in that the traditional unity-gain buffer output stage is not used; instead, the output is taken directly from the output of the integrator, to allow rail-to-rail output swing. Since the buffer traditionally delivers the power to the load, while maintaining high op amp gain and stability, and must withstand shorts to either rail, these tasks now fall to the integrator.

As a result of these demands, the integrator is a compound affair with an embedded gain stage that is doubly fed forward (via C_f and C_{ff}) by a dedicated unity-gain compensation driver. In addition, the output portion of the integrator is a push-pull configuration for delivering heavy loads. While sinking current the whole amplifier path consists of three gain stages with one stage fed forward, whereas while sourcing the path contains four gain stages with two fed forward.

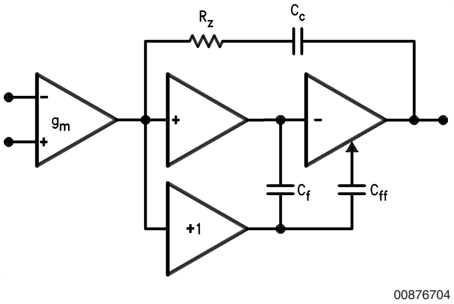


FIGURE 1. LMC660 Circuit Topology (Each Amplifier)

The large signal voltage gain while sourcing is comparable to traditional bipolar op amps, even with a 600Ω load. The gain while sinking is higher than most CMOS op amps, due to the additional gain stage; however, under heavy load (600Ω) the gain will be reduced as indicated in the Electrical Characteristics. Avoid resistive loads of less than 500Ω, as they may cause instability.

COMPENSATING INPUT CAPACITANCE

The high input resistance of the LMC660 op amps allows the use of large feedback and source resistor values without losing gain accuracy due to loading. However, the circuit will be especially sensitive to its layout when these large-value resistors are used.

Every amplifier has some capacitance between each input and AC ground, and also some differential capacitance between the inputs. When the feedback network around an amplifier is resistive, this input capacitance (along with any additional capacitance due to circuit board traces, the socket, etc.) and the feedback resistors create a pole in the feedback path. In the following General Operational Amplifier circuit,*Figure 2* the frequency of this pole is

$$fp = \frac{1}{2\pi C_S R_P}$$

where C_S is the total capacitance at the inverting input, including amplifier input capacitance and any stray capacitance from the IC socket (if one is used), circuit board traces, etc., and R_P is the parallel combination of R_F and R_{IN}. This formula, as well as all formulae derived below, apply to inverting and non-inverting op amp configurations.

When the feedback resistors are smaller than a few kΩ, the frequency of the feedback pole will be quite high, since C_S is generally less than 10 pF. If the frequency of the feedback pole is much higher than the "ideal" closed-loop bandwidth (the nominal closed-loop bandwidth in the absence of C_S), the pole will have a negligible effect on stability, as it will add only a small amount of phase shift.

However, if the feedback pole is less than approximately 6 to 10 times the "ideal" −3 dB frequency, a feedback capacitor, C_F, should be connected between the output and the inverting input of the op amp. This condition can also be stated in terms of the amplifier's low-frequency noise gain: To maintain stability a feedback capacitor will probably be needed if

$$\left(\frac{R_F}{R_{IN}} + 1\right) \leq \sqrt{6 \times 2\pi \times GBW \times R_F \times C_S}$$

where

$$\left(\frac{R_F}{R_{IN}} + 1\right)$$

is the amplifier's low-frequency noise gain and GBW is the amplifier's gain bandwidth product. An amplifier's low-frequency noise gain is represented by the formula

$$\left(\frac{R_F}{R_{IN}} + 1\right)$$

regardless of whether the amplifier is being used in inverting or non-inverting mode. Note that a feedback capacitor is more likely to be needed when the noise gain is low and/or the feedback resistor is large.

If the above condition is met (indicating a feedback capacitor will probably be needed), and the noise gain is large enough that:

$$\left(\frac{R_F}{R_{IN}} + 1\right) \geq 2\sqrt{GBW \times R_F \times C_S},$$

the following value of feedback capacitor is recommended:

$$C_F = \frac{C_S}{2\left(\frac{R_F}{R_{IN}} + 1\right)}$$

If

$$\left(\frac{R_F}{R_{IN}} + 1\right) < 2\sqrt{GBW \times R_F \times C_S}$$

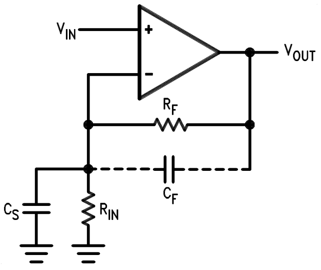
the feedback capacitor should be:

$$C_F = \sqrt{\frac{C_S}{GBW \times R_F}}$$

Application Hints (Continued)

Note that these capacitor values are usually significant smaller than those given by the older, more conservative formula:

$$C_F = \frac{C_S R_{IN}}{R_F}$$



C_S consists of the amplifier's input capacitance plus any stray capacitance from the circuit board and socket. C_F compensates for the pole caused by C_S and the feedback resistors.

FIGURE 2. General Operational Amplifier Circuit

Using the smaller capacitors will give much higher bandwidth with little degradation of transient response. It may be necessary in any of the above cases to use a somewhat larger feedback capacitor to allow for unexpected stray capacitance, or to tolerate additional phase shifts in the loop, or excessive capacitive load, or to decrease the noise or bandwidth, or simply because the particular circuit implementation needs more feedback capacitance to be sufficiently stable. For example, a printed circuit board's stray capacitance may be larger or smaller than the breadboard's, so the actual optimum value for C_F may be different from the one estimated using the breadboard. In most cases, the values of C_F should be checked on the actual circuit, starting with the computed value.

CAPACITIVE LOAD TOLERANCE

Like many other op amps, the LMC660 may oscillate when its applied load appears capacitive. The threshold of oscillation varies both with load and circuit gain. The configuration most sensitive to oscillation is a unity-gain follower. See Typical Performance Characteristics.

The load capacitance interacts with the op amp's output resistance to create an additional pole. If this pole frequency is sufficiently low, it will degrade the op amp's phase margin so that the amplifier is no longer stable at low gains. As shown in *Figure 3*, the addition of a small resistor (50Ω to 100Ω) in series with the op amp's output, and a capacitor (5 pF to 10 pF) from inverting input to output pins, returns the phase margin to a safe value without interfering with lower-frequency circuit operation. Thus larger values of capacitance can be tolerated without oscillation. Note that in all cases, the output will ring heavily when the load capacitance is near the threshold for oscillation.

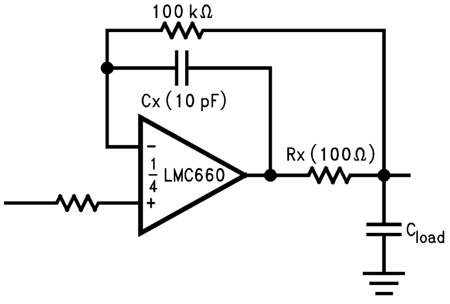


FIGURE 3. Rx, Cx Improve Capacitive Load Tolerance

Capacitive load driving capability is enhanced by using a pull up resistor to V^+ (*Figure 4*). Typically a pull up resistor conducting 500 μA or more will significantly improve capacitive load responses. The value of the pull up resistor must be determined based on the current sinking capability of the amplifier with respect to the desired output swing. Open loop gain of the amplifier can also be affected by the pull up resistor (see Electrical Characteristics).

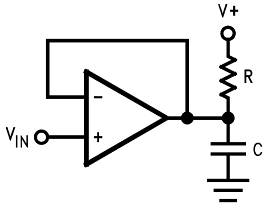


FIGURE 4. Compensating for Large Capacitive Loads with a Pull Up Resistor

PRINTED-CIRCUIT-BOARD LAYOUT FOR HIGH-IMPEDANCE WORK

It is generally recognized that any circuit which must operate with less than 1000 pA of leakage current requires special layout of the PC board. When one wishes to take advantage of the ultra-low bias current of the LMC662, typically less than 0.04 pA, it is essential to have an excellent layout. Fortunately, the techniques for obtaining low leakages are quite simple. First, the user must not ignore the surface leakage of the PC board, even though it may sometimes appear acceptably low, because under conditions of high humidity or dust or contamination, the surface leakage will be appreciable.

To minimize the effect of any surface leakage, lay out a ring of foil completely surrounding the LMC660's inputs and the terminals of capacitors, diodes, conductors, resistors, relay terminals, etc. connected to the op amp's inputs. See*Figure* 5. To have a significant effect, guard rings should be placed on both the top and bottom of the PC board. This PC foil must then be connected to a voltage which is at the same voltage as the amplifier inputs, since no leakage current can flow between two points at the same potential. For example, a PC board trace-to-pad resistance of $10^{12}\Omega$, which is normally considered a very large resistance, could leak 5 pA if the trace were a 5V bus adjacent to the pad of an input. This would cause a 100 times degradation from the LMC660's actual performance. However, if a guard ring is held within 5 mV of the inputs, then even a resistance of $10^{11}\Omega$ would

Application Hints (Continued)

cause only 0.05 pA of leakage current, or perhaps a minor (2:1) degradation of the amplifier's performance. See *Figure 6a*,*Figure 6b*, *Figure 6c* for typical connections of guard rings for standard op amp configurations. If both inputs are active and at high impedance, the guard can be tied to ground and still provide some protection; see *Figure 6d*.

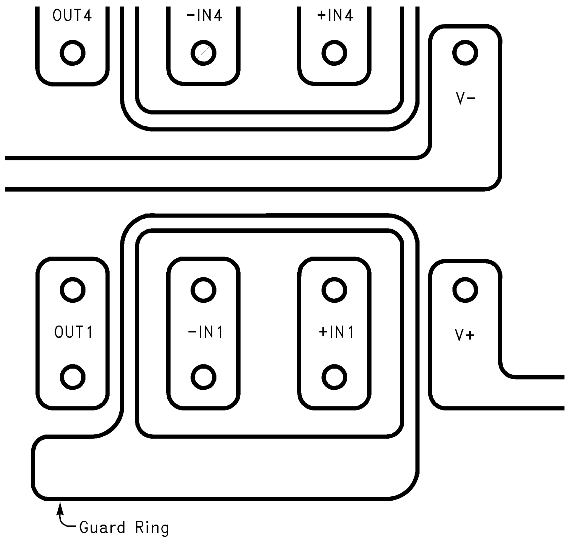


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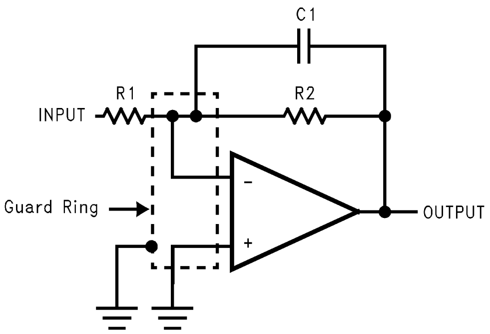
FIGURE 5. Example, using the LMC660, of Guard Ring in P.C. Board Layout



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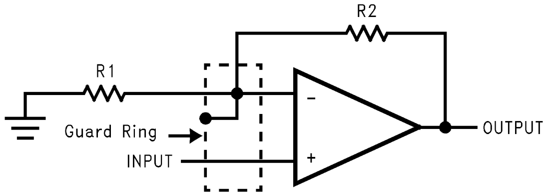
(a) Inverting Amplifier



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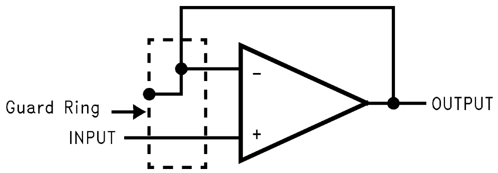
(b) Non-Inverting Amplifier



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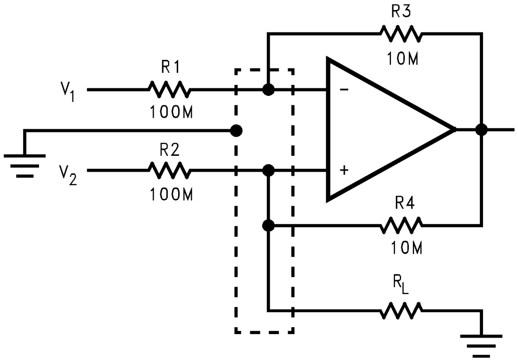
(c) Follower



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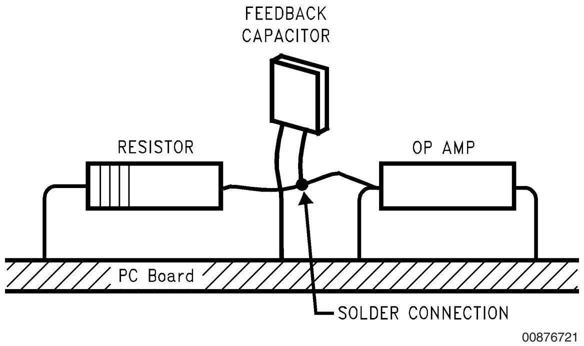
(d) Howland Current Pump

FIGURE 6. Guard Ring Connections

The designer should be aware that when it is inappropriate to lay out a PC board for the sake of just a few circuits, there is another technique which is even better than a guard ring on a PC board: Don't insert the amplifier's input pin into the board at all, but bend it up in the air and use only air as an insulator. Air is an excellent insulator. In this case you may have to forego some of the advantages of PC board construction, but the advantages are sometimes well worth the effort of using point-to-point up-in-the-air wiring. See *Figure 7*.

Application Hints (Continued)



(Input pins are lifted out of PC board and soldered directly to components. All other pins connected to PC board.)

FIGURE 7. Air Wiring

BIAS CURRENT TESTING

The test method of *Figure 7* is appropriate for bench-testing bias current with reasonable accuracy. To understand its operation, first close switch S2 momentarily. When S2 is opened, then

$$I_b{}^- = \frac{dV_{OUT}}{dt} \times C2.$$

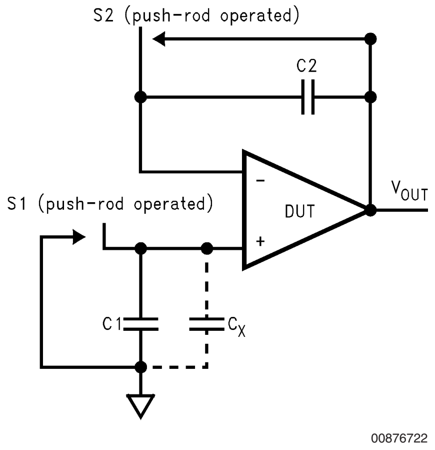


FIGURE 8. Simple Input Bias Current Test Circuit

A suitable capacitor for C2 would be a 5 pF or 10 pF silver mica, NPO ceramic, or air-dielectric. When determining the magnitude of I_b-, the leakage of the capacitor and socket must be taken into account. Switch S2 should be left shorted most of the time, or else the dielectric absorption of the capacitor C2 could cause errors.

Similarly, if S1 is shorted momentarily (while leaving S2 shorted)

$$I_b{}^+ = \frac{dV_{OUT}}{dt} \times (C1 + C_x)$$

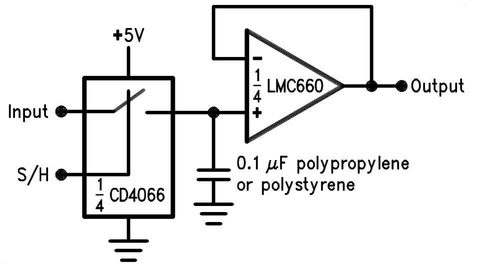
where C_x is the stray capacitance at the + input.

Typical Single-Supply Applications

(V^+ = 5.0 VDC)

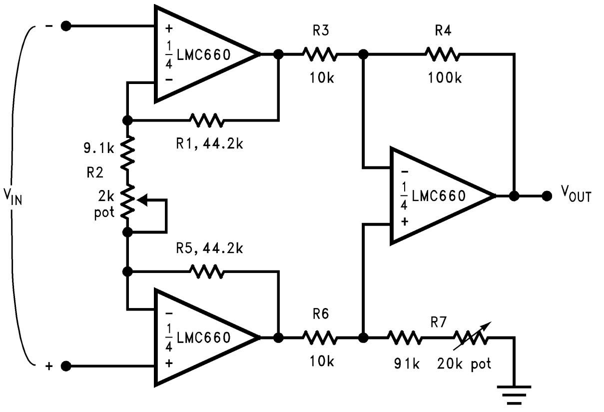
Additional single-supply applications ideas can be found in the LM324 datasheet. The LMC660 is pin-for-pin compatible with the LM324 and offers greater bandwidth and input resistance over the LM324. These features will improve the performance of many existing single-supply applications. Note, however, that the supply voltage range of the LMC660 is smaller than that of the LM324.

Low-Leakage Sample-and-Hold



00876707

Instrumentation Amplifier



00876708

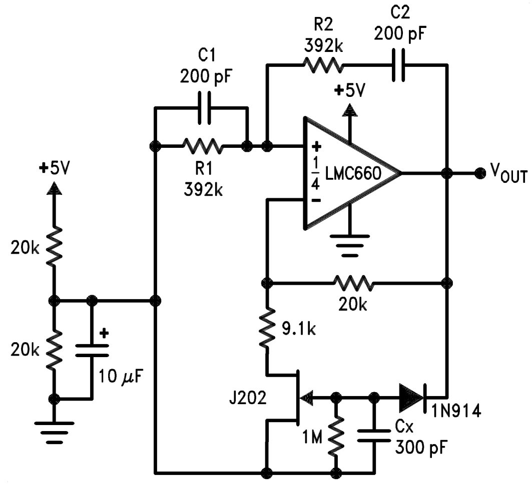
If R1 = R5, R3 = R6, and R4 = R7; then

$$\frac{V_{OUT}}{V_{IN}} = \frac{R2 + 2R1}{R2} \times \frac{R4}{R3}$$

∴ $A_V \approx 100$ for circuit shown.

For good CMRR over temperature, low drift resistors should be used. Matching of R3 to R6 and R4 to R7 affect CMRR. Gain may be adjusted through R2. CMRR may be adjusted through R7.

Sine-Wave Oscillator



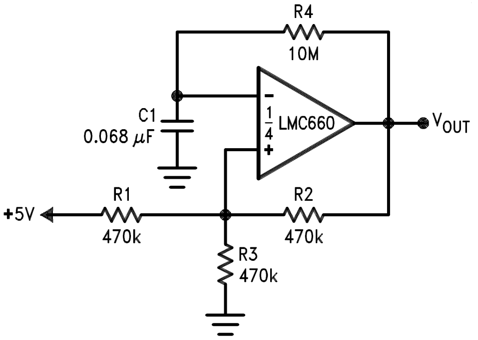
00876709

Oscillator frequency is determined by R1, R2, C1, and C2:

fosc = 1/2πRC, where R = R1 = R2 and C = C1 = C2.

This circuit, as shown, oscillates at 2.0 kHz with a peak-to-peak output swing of 4.5V.

1 Hz Square-Wave Oscillator



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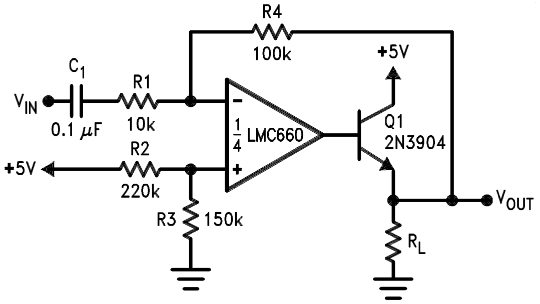
Power Amplifier

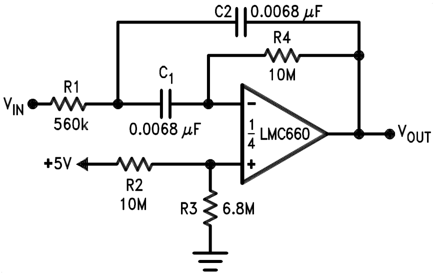


00876711

Typical Single-Supply Applications

(V+ = 5.0 VDC) (Continued)

10 Hz Bandpass Filter



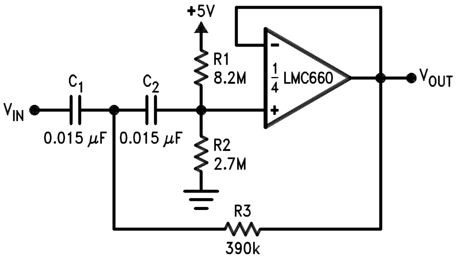
00876712

f_O = 10 Hz

Q = 2.1

Gain = −8.8

10 Hz High-Pass Filter



00876713

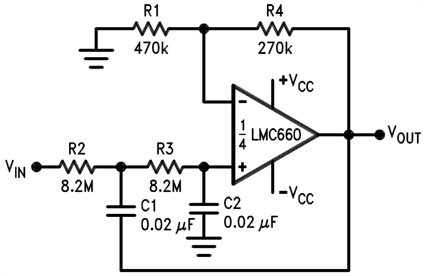
f_c = 10 Hz

d = 0.895

Gain = 1

2 dB passband ripple

1 Hz Low-Pass Filter (Maximally Flat, Dual Supply Only)



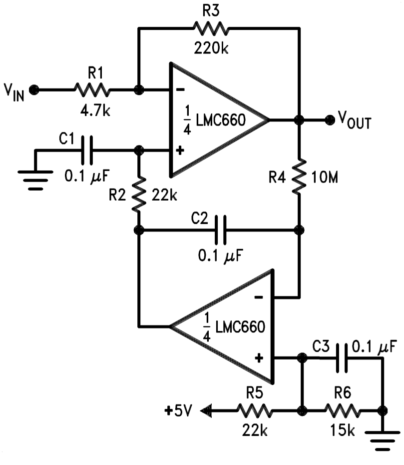
00876714

f_c = 1 Hz

d = 1.414

Gain = 1.57

High Gain Amplifier with Offset Voltage Reduction

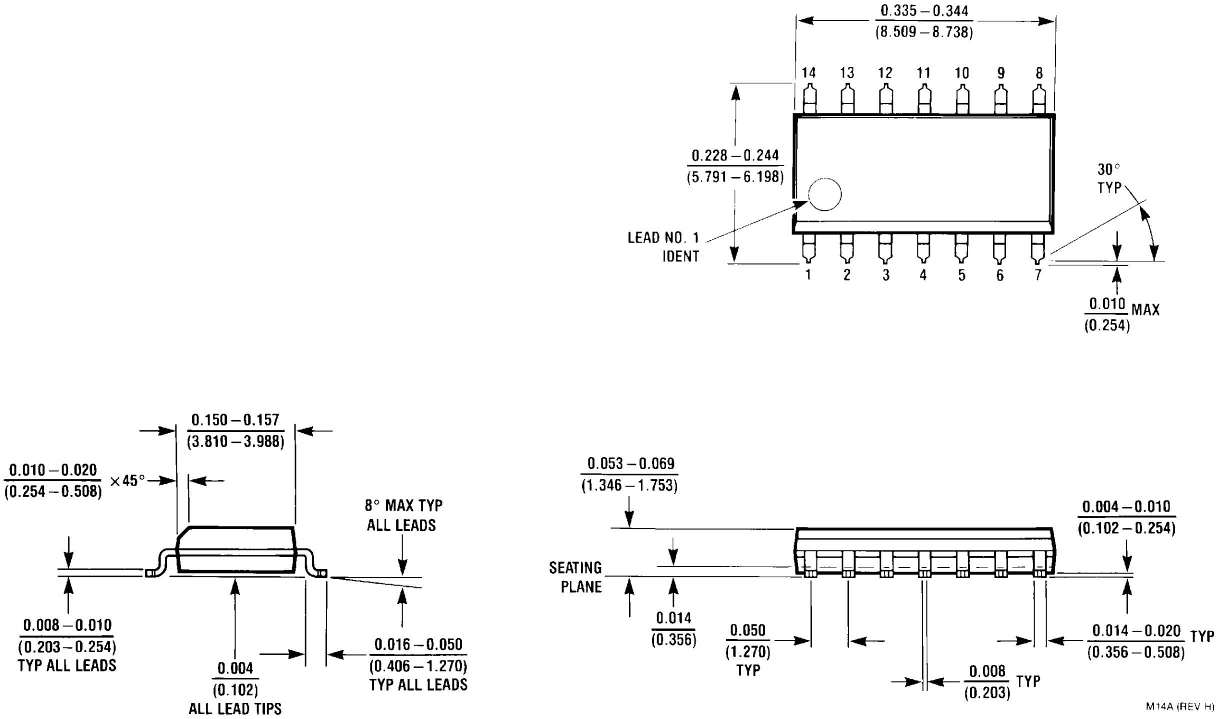


00876715

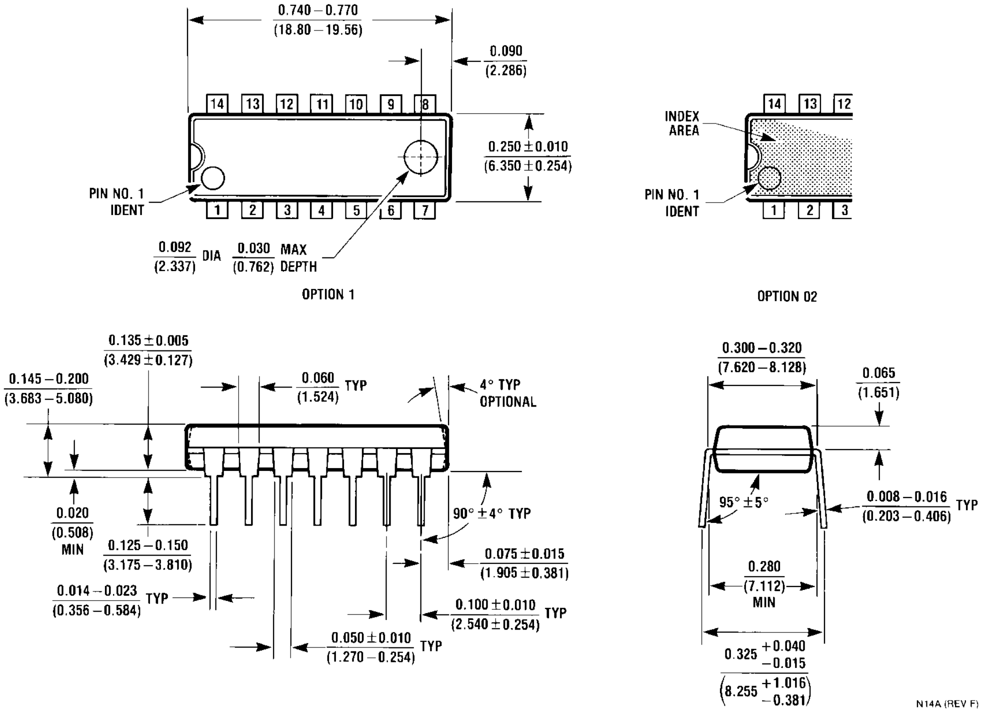
Gain = −46.8

Output offset voltage reduced to the level of the input offset voltage of the bottom amplifier (typically 1 mV).

Physical Dimensions inches (millimeters) unless otherwise noted



14-Pin SOIC
NS Package Number M14A



14-Pin MDIP
NS Package Number N14A

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