

## SN7546x Darlington Transistor Arrays

### 1 Features

- 500-mA Rated Collector Current (Single Output)
- High-Voltage Output 100 V
- Output Clamp Diodes
- Inputs Compatible With Various Types of Logic
- Relay Driver Applications
- Higher-Voltage Versions of ULN2003A and ULN2004A, for Commercial Temperature range

### 2 Applications

- Relay Drivers
- Hammer Drivers
- Lamp Drivers
- Display Drivers (LED and Gas Discharge)
- Line Drivers
- Logic Buffers

### 3 Description

The SN75468 and SN75469 are high-voltage, high-current Darlington transistor arrays. Each consists of seven NPN Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers.

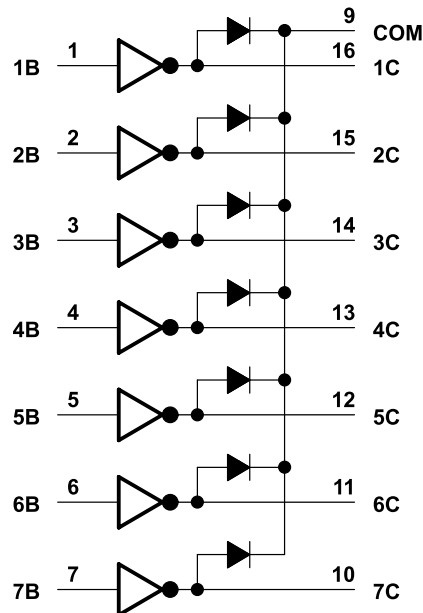
The SN75468 has a 2700- $\Omega$  series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS. The SN75469 has a 10.5-k $\Omega$  series base resistor to allow its operation directly with CMOS or PMOS that use supply voltages of 6 to 15 V. The required input current is below that of the SN75468.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
SN7546x	D (16)	9.90 mm x 3.91 mm
	N (16)	19.30 mm x 6.35 mm
	NS (16)	10.30 mm x 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

### 4 Simplified Schematic



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## 5 Revision History

### Changes from Revision D (November 2004) to Revision E

Page

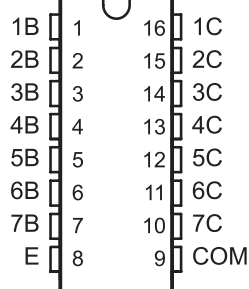
<ul style="list-style-type: none"> <li>Added <i>Applications</i>, <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i>, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section. ....</li> <li>Deleted <i>Ordering Information</i> table. ....</li> </ul>	<b>1</b>
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## 6 Pin Configuration and Functions

SN75468 . . . D, N, OR NS PACKAGE

SN75469 . . . D OR N PACKAGE

(TOP VIEW)



### Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
<1:7>B	1 - 7	I	Channel 1 through 7 darlington base input
<1:7>C	16 - 10	O	Channel 1 through 7 darlington collector output
E	7	—	Common Emmitter shared by all channels (typically tied to ground)
COM	8	I/O	Common cathode node for flyback diodes (required for inductive loads)

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CE}$	Collector-emitter voltage		100	V
$V_I$	Input voltage <sup>(2)</sup>		30	V
	Peak collector current		500	mA
$I_{OK}$	Output clamp current		500	mA
	Total emitter-terminal current		-2.5	A
$T_J$	Operating virtual junction temperature		150	°C
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

### 7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_I$		0	5	V
$V_{CC}$		0	100	V
$T_J$	Junction Temperature	-40	125	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN7546x	UNIT
		D	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	40.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	38.9	
$\Psi_{JT}$	Junction-to-top characterization parameter	10.9	
$\Psi_{JB}$	Junction-to-board characterization parameter	38.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

 $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS <sup>(1)</sup>	SN75468			SN75469			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$V_{I(on)}$ On-state input voltage	$V_{CE} = 2\text{ V}$	$I_C = 125\text{ mA}$						V
		$I_C = 200\text{ mA}$		2.4				
		$I_C = 250\text{ mA}$			2.7			
		$I_C = 275\text{ mA}$						
		$I_C = 300\text{ mA}$			3			
		$I_C = 350\text{ mA}$						
$V_{CE(sat)}$ Collector-emitter saturation voltage	$I_I = 250\text{ }\mu\text{A}, I_C = 100\text{ mA}$		0.9	1.1	0.9	1.1	V	
	$I_I = 350\text{ }\mu\text{A}, I_C = 100\text{ mA}$		1	1.3	1	1.3		
	$I_I = 500\text{ }\mu\text{A}, I_C = 100\text{ mA}$		1.2	1.6	1.2	1.6		
$V_F$ Clamp-diode forward voltage	$I_F = 350\text{ mA}$		1.7	2	1.7	2	V	
$I_{CEX}$ collector cutoff current	$V_{CE} = 100\text{ V}, I_I = 0$			50		50	$\mu\text{A}$	
	$V_{CE} = 100\text{ V}, T_A = 70^\circ\text{C}$	$I_I = 0$		100		100		
		$V_I = 1\text{ V}$				500		
$I_{I(off)}$ Off-state input current	$V_{CE} = 50\text{ V}, I_C = 500\text{ }\mu\text{A}, T_A = 70^\circ\text{C}$	50	65		50	65	$\mu\text{A}$	
$I_I$ Input current	$V_I = 3.85\text{ V}$		0.93	1.35			mA	
	$V_I = 5\text{ V}$				0.35	0.5		
	$V_I = 12\text{ V}$				1	1.45		
$I_R$ Clamp-diode reverse current	$V_R = 100\text{ V}$			50		50	$\mu\text{A}$	
	$V_R = 100\text{ V}, T_A = 70^\circ\text{C}$			100		10		
$C_i$ Input Capacitance	$V_I = 0, f = 1\text{ MHz}$		15	25		15	25	pF

(1) All electrical characteristics are measured with 0.1- $\mu\text{F}$  capacitors connected at REF, CT, and  $V_{CC}$  to GND.

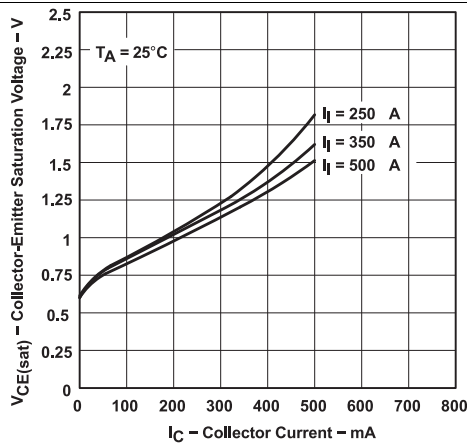
## 7.6 Switching Characteristics

 $T_A = 25^\circ\text{C}$  free-air temperature

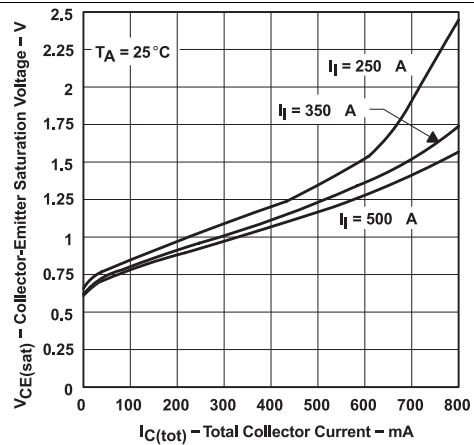
PARAMETER	TEST CONDITIONS <sup>(1)</sup>	MIN	TYP	MAX	UNIT
$t_{PLH}$ Propagation delay time, low-to-high-level output	$V_S = 20\text{ V}, R_L = 163\text{ }\Omega, C_L = 15\text{ pF}$ , See <a href="#">Figure 14</a>		0.25	1	$\mu\text{s}$
$t_{PHL}$ Propagation delay time, high-to-low-level output			0.25	1	$\mu\text{s}$
$V_{OH}$ High-level output voltage after switching	$V_S = 50\text{ V}, I_O = 300\text{ mA}$ , See <a href="#">Figure 14</a>	$V_S - 20$			mV

(1) All switching characteristics are measured with 0.1- $\mu\text{F}$  capacitors connected at REF and  $V_{CC}$  to GND.

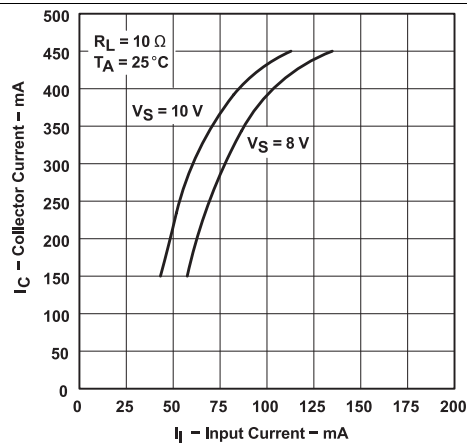
### 7.7 Typical Characteristics



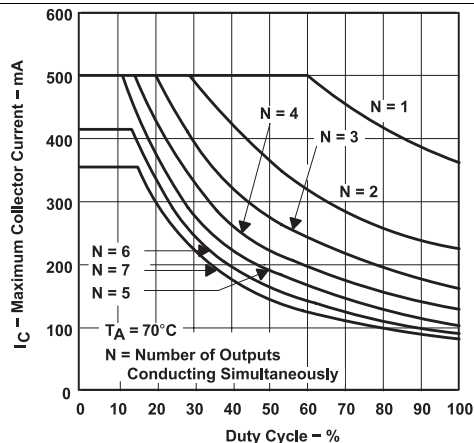
**Figure 1. Collector-Emitter Saturation Voltage vs Collector Current (One Darlington)**



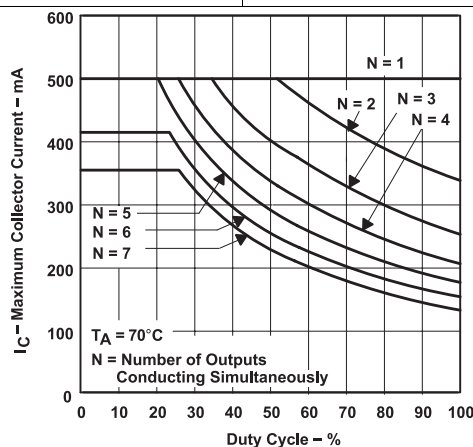
**Figure 2. Collector-Emitter Saturation Voltage vs Total Collector Current (Two Darlington in Parallel)**



**Figure 3. Output Current vs Input Current**



**Figure 4. D Package Maximum Collector Current vs Duty Cycle**



**Figure 5. N Package Maximum Collector Current vs Duty Cycle**

## 8 Parameter Measurement Information

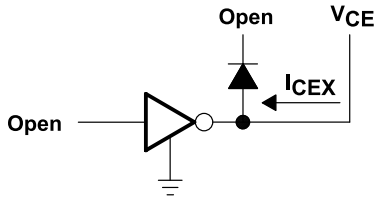


Figure 6.  $I_{CEX}$

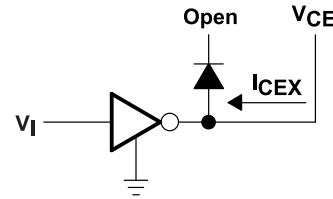


Figure 7.  $I_{CES}$

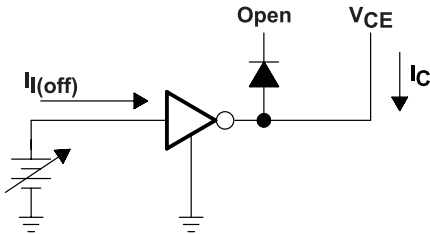


Figure 8.  $I_{I(off)}$

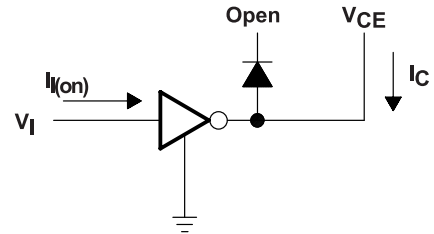


Figure 9.  $I_I$

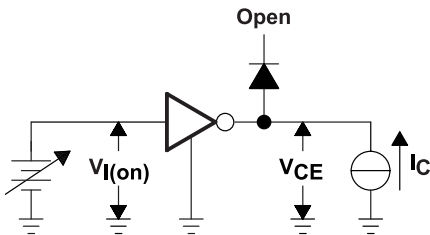


Figure 10.  $V_{I(on)}$

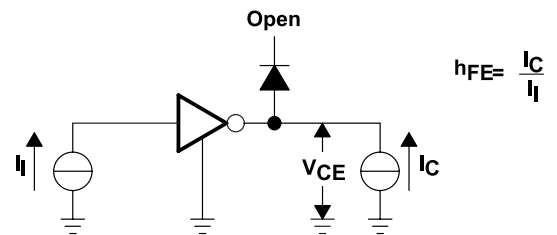


Figure 11.  $h_{FE}$ ,  $V_{CE(sat)}$

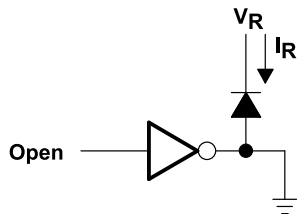


Figure 12.  $I_R$

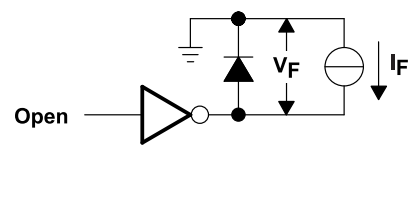
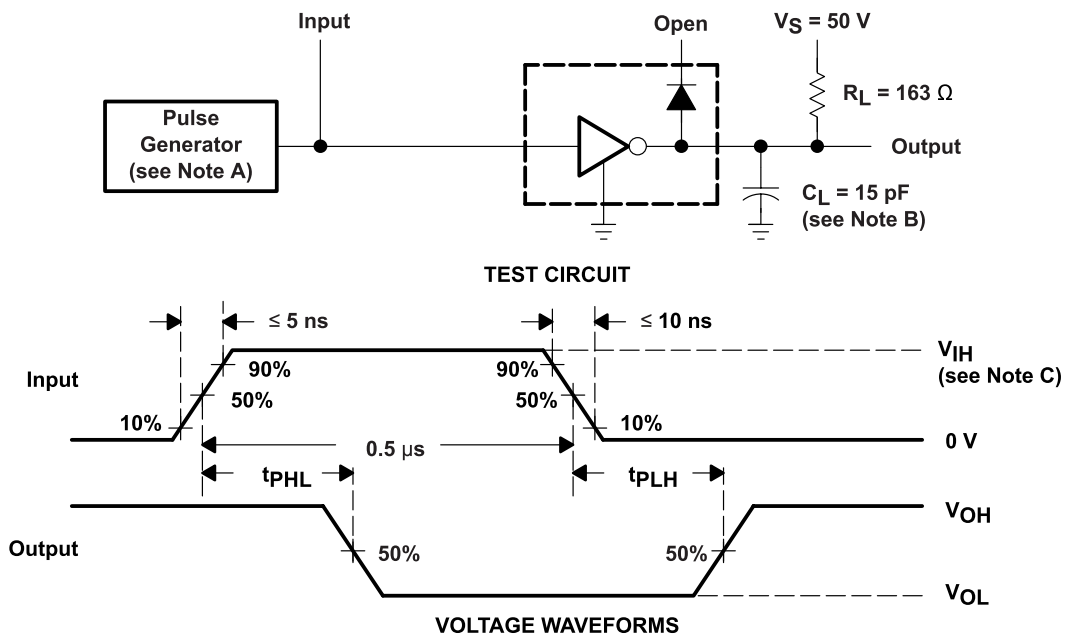


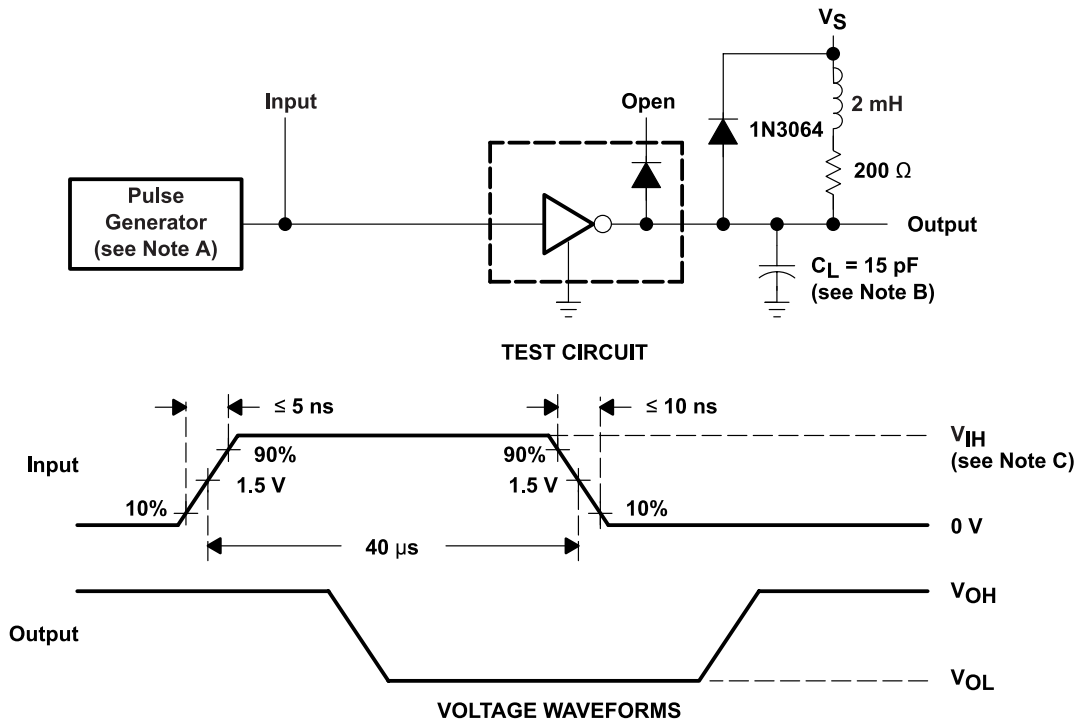
Figure 13.  $V_F$

**Parameter Measurement Information (continued)**



- A. The pulse generator has the following characteristics: PRR = 12.5 kHz,  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes probe and jig capacitance.
- C. For testing the '468,  $V_{IH} = 3 \text{ V}$ ; for the '469,  $V_{IH} = 8 \text{ V}$ .

**Figure 14. Test Circuit and Voltage Waveforms**



- A. The pulse generator has the following characteristics: PRR = 12.5 kHz,  $Z_O = 50 \Omega$ .
- B.  $C_L$  includes probe and jig capacitance.
- C. For testing the '468,  $V_{IH} = 3 \text{ V}$ ; for the '469,  $V_{IH} = 8 \text{ V}$ .

**Figure 15. Latch-Up Test Circuit and Voltage Waveforms**





## 10 Application and Implementation

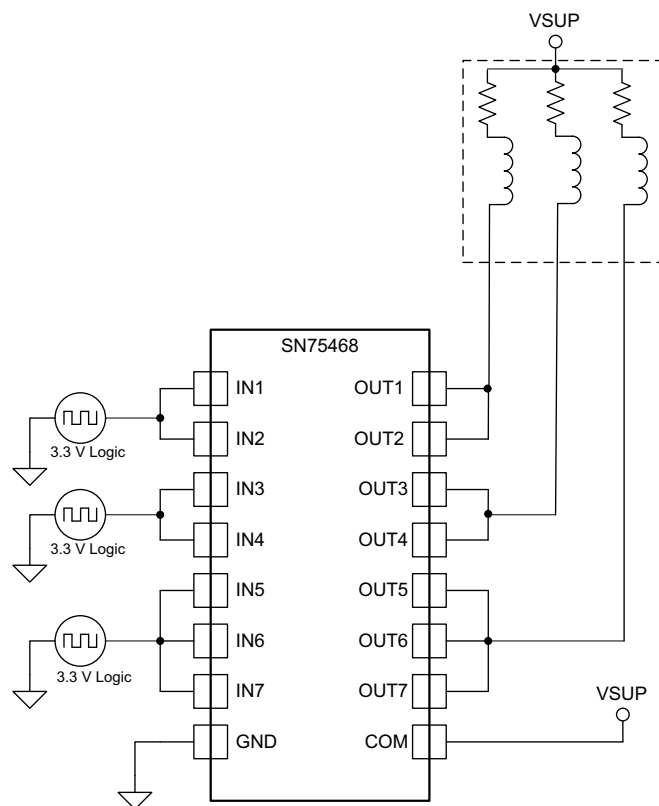
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

SN75468 will typically be used to drive a high voltage and/or current peripheral from an MCU or logic device that cannot tolerate these conditions. The following design is a common application of SN75468, driving inductive loads. This includes motors, solenoids & relays. Each load type can be modeled by what's seen in [Figure 16](#).

### 10.2 Typical Application



**Figure 16. SN75468 as Inductive Load Driver**

#### 10.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) as the input parameters.

**Table 1. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
GPIO Voltage	3.3 V or 5.0 V
Coil Supply Voltage	12 V to 100 V
Number of Channels	7
Output Current ( $R_{COIL}$ )	20 mA to 300 mA per channel
Duty Cycle	100%

## 10.2.2 Detailed Design Procedure

When using SN75468 in a coil driving application, determine the following:

- Input voltage range
- Temperature range
- Output and drive current
- Power dissipation

### 10.2.2.1 Drive Current

The coil current is determined by the coil voltage ( $V_{SUP}$ ), coil resistance & output low voltage ( $V_{OL}$  or  $V_{CE(SAT)}$ ).

$$I_{COIL} = (V_{SUP} - V_{CE(SAT)}) / R_{COIL} \quad (1)$$

### 10.2.2.2 Output Low Voltage

The output low voltage ( $V_{OL}$ ) is the same thing as  $V_{CE(SAT)}$  and can be determined by the [Electrical Characteristics](#) table, [Figure 1](#), or [Figure 2](#).

### 10.2.2.3 Power Dissipation & Temperature

The number of coils driven is dependent on the coil current and on-chip power dissipation. The number of coils driven can be determined by [Figure 4](#) or [Figure 5](#).

For a more accurate determination of number of coils possible, use the below equation to calculate SN75468 on-chip power dissipation  $P_D$ :

$$P_D = \sum_{i=1}^N V_{OLi} \times I_{Li}$$

Where:

$N$  is the number of channels active together.

$V_{OLi}$  is the  $OUT_i$  pin voltage for the load current  $I_{Li}$ . This is the same as  $V_{CE(SAT)}$  (2)

In order to guarantee reliability of SN75468 and the system the on-chip power dissipation must be lower than or equal to the maximum allowable power dissipation ( $PD_{(MAX)}$ ) dictated by below equation [Equation 3](#).

$$PD_{(MAX)} = \frac{(T_{J(MAX)} - T_A)}{\theta_{JA}}$$

Where:

$T_{J(MAX)}$  is the target maximum junction temperature.

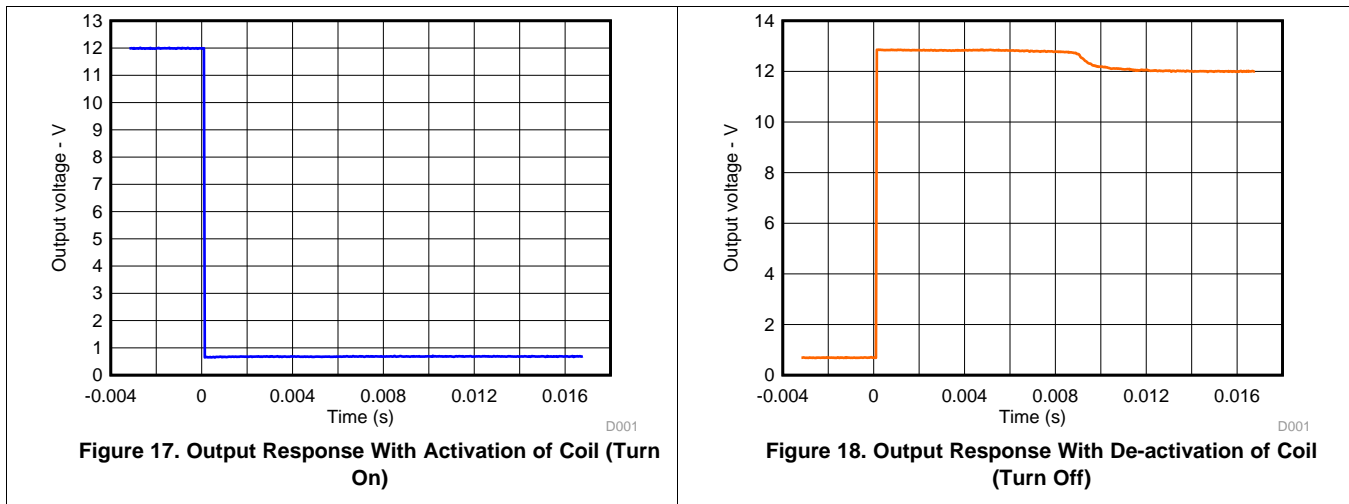
$T_A$  is the operating ambient temperature.

$\theta_{JA}$  is the package junction to ambient thermal resistance. (3)

It is recommended to limit SN75468 IC's die junction temperature to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation.

### 10.2.3 Application Curves

The following curves were generated with SN75468 driving an OMRON G5NB relay –  $V_{in} = 5.0V$ ;  $V_{sup} = 12 V$  &  $R_{COIL} = 2.8 k\Omega$



### 10.3 System Examples

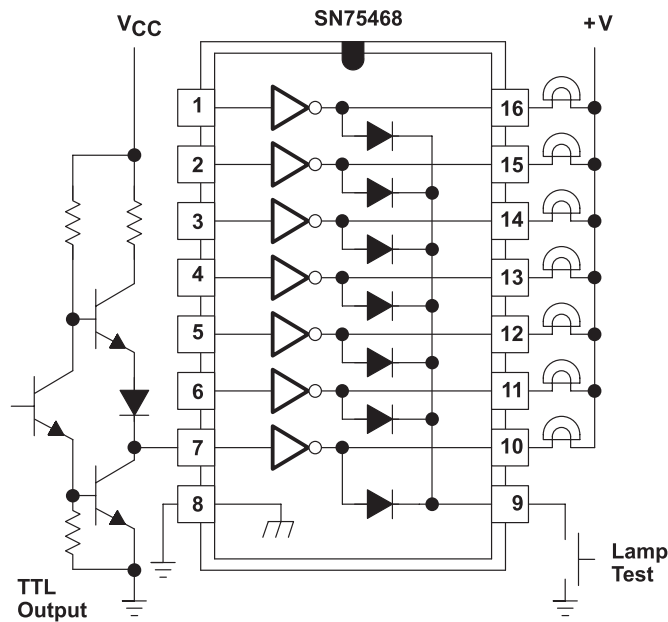


Figure 19. TTL to Load Schematic

System Examples (continued)

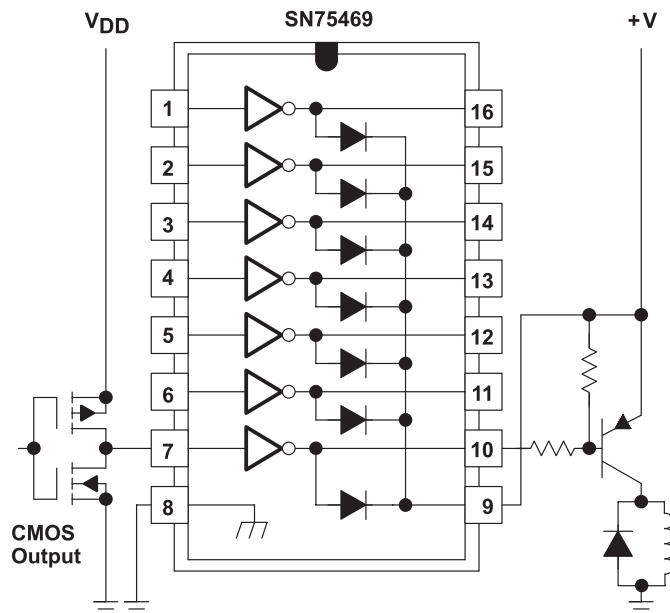


Figure 20. Buffer to Higher Current Loads Schematic

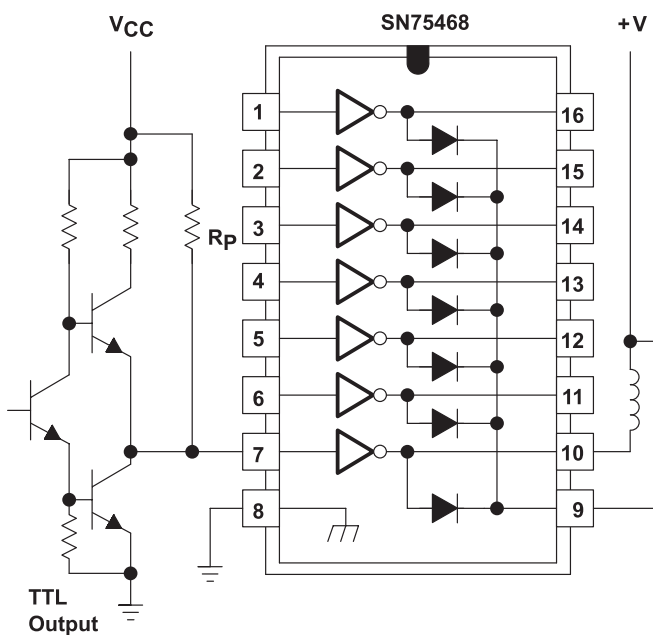


Figure 21. Pull-up Resistor Schematic

## 11 Power Supply Recommendations

This part does not need a power supply; however, the COM pin is typically tied to the system power supply. When this is the case, it is very important to make sure that the output voltage does not heavily exceed the COM pin voltage. This will heavily forward bias the fly-back diodes and cause a large current to flow into COM, potentially damaging the on-chip metal or over-heating the part.

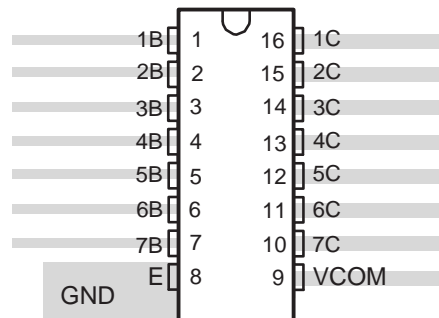
## 12 Layout

### 12.1 Layout Guidelines

Thin traces can be used on the input due to the low current logic that is typically used to drive SN75468. Care must be taken to separate the input channels as much as possible, as to eliminate cross-talk. Thick traces are recommended for the output, in order to drive whatever high currents that may be needed. Wire thickness can be determined by the trace material's current density and desired drive current.

Since all of the channels currents return to a common emitter, it is best to size that trace width to be very wide. Some applications require up to 2.5 A.

### 12.2 Layout Example



**Figure 22. Package Layout**

## 13 Device and Documentation Support

### 13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN75468	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SN75469	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 13.2 Trademarks

All trademarks are the property of their respective owners.

### 13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75468D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75468	<a href="#">Samples</a>
SN75468DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75468	<a href="#">Samples</a>
SN75468DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75468	<a href="#">Samples</a>
SN75468DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75468	<a href="#">Samples</a>
SN75468N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75468N	<a href="#">Samples</a>
SN75468NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75468N	<a href="#">Samples</a>
SN75468NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75468	<a href="#">Samples</a>
SN75468NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75468	<a href="#">Samples</a>
SN75469D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75469	<a href="#">Samples</a>
SN75469DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75469	<a href="#">Samples</a>
SN75469DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75469	<a href="#">Samples</a>
SN75469DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75469	<a href="#">Samples</a>
SN75469N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75469N	<a href="#">Samples</a>
SN75469NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75469N	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.



<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75469DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75469DR	SOIC	D	16	2500	333.2	345.9	28.6

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

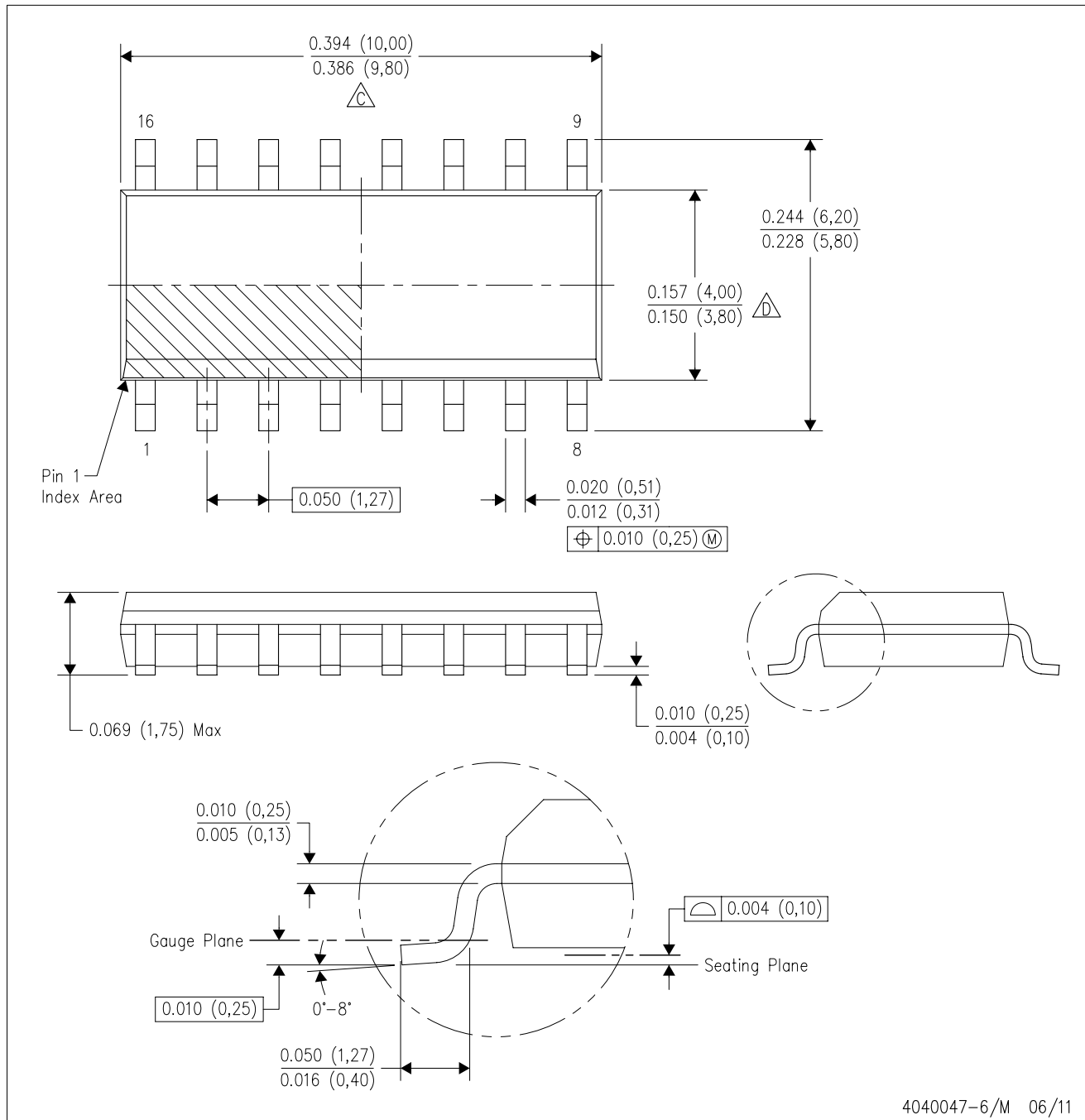
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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