DS3691 (RS-422/RS-423) Line Drivers with TRI-STATE Outputs

Check for Samples: DS1691A, DS3691

FEATURES

- **Dual RS-422 Line Driver with Mode Pin Low, or Quad RS-423 Line Driver with Mode Pin High**
- **TRI-STATE Outputs in RS-422 Mode**
- **Short Circuit Protection for Both Source and Sink Outputs**
- **Outputs Will Not Clamp Line with Power Off or In TRI-STATE**
- **100Ω Transmission Line Drive Capability**
- **Low I_{CC} and I_{EE} Power Consumption**
  - **RS-422: I_{CC} = 9 mA/driver Typ**
  - **RS-423: I_{CC} = 4.5 mA/driver Typ**
  - **I_{EE} = 2.5 mA/driver Typ**
- **Low Current PNP Inputs Compatible with TTL, MOS and CMOS**
- **Pin Compatible with AM26LS30**

DESCRIPTION

The DS3691 is a low power Schottky TTL line driver designed to meet the requirements of EIA standards RS-422 and RS-423. It features 4 buffered outputs with high source and sink current capability with internal short circuit protection. A mode control input provides a choice of operation either as 4 single-ended line drivers or 2 differential line drivers. A rise time control pin allows the use of an external capacitor to slow the rise time for suppression of near end crosstalk to other receivers in the cable. Rise time capacitors are primarily intended for waveshaping output signals in the single-ended driver mode. Multipoint applications in differential mode with waveshaping capacitors is not allowed.

With the mode select pin low, the DS3691 are dual-differential line drivers with TRI-STATE outputs. They feature ±10V output common-mode range in TRI-STATE mode and 0V output unbalance when operated with ±5V supply.

Connection Diagrams

With Mode Select LOW (RS-422 Connection)

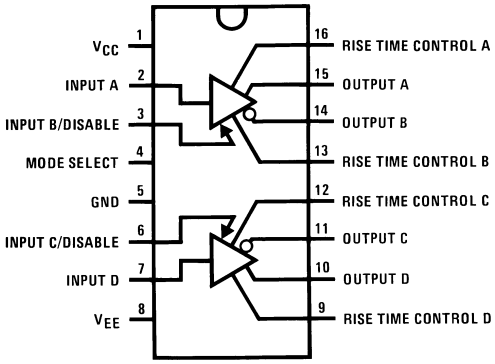


Figure 1. SOIC Package
See Package Number D0016A
Top View

With Mode Select HIGH (RS-423 Connection)

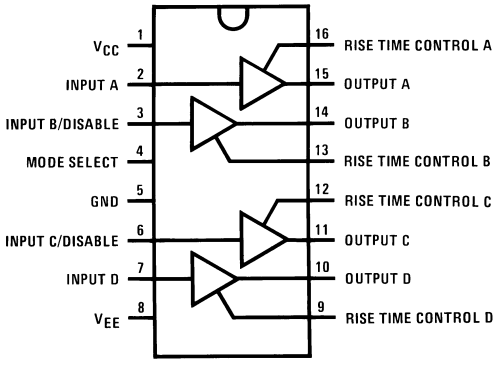


Figure 2. SOIC Package
See Package Number D0016A
Top View

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings[1][2]

Supply Voltage	V_{CC}	7V
	V_{EE}	−7V
Maximum Power Dissipation at 25°C SOIC Package[3]		1051 mW
Input Voltage		15V
Output Voltage (Power OFF)		±15V
Storage Temperature		−65°C to + 150°C
Lead Temperature (Soldering, 4 seconds)		260°C

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be verified. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" provide conditions for actual device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Derate SOIC package 8.41 mW/°C above 25°C.

Operating Conditions

		Min	Max	Units
Supply Voltage	V_{CC}	4.75	5.25	V
	V_{EE}	−4.75	−5.25	V
Temperature, T_A		0	+70	°C

DC Electrical Characteristics[1][2][3][4]

Parameter		Test Conditions		Min	Typ	Max	Units
RS-422 CONNECTION, V_{EE} CONNECTION TO GROUND, MODE SELECT ≤ 0.8V							
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	V_{IN} = 2.4V			1	40	µA
		V_{IN} ≤ 15V			10	100	µA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			−30	−200	µA
V_I	Input Clamp Voltage	I_{IN} = −12 mA				−1.5	V
V_O	Differential Output Voltage $V_{A,B}$	R_L = ∞	V_{IN} = 2V		3.6	6.0	V
$\overline{V_O}$			V_{IN} = 0.8V		−3.6	−6.0	V
V_T	Differential Output Voltage $V_{A,B}$	R_L = 100Ω, V_{CC} ≥ 4.75V	V_{IN} = 2V	2	2.4		V
$\overline{V_T}$			V_{IN} = 0.8V	−2	−2.4		V
V_{OS}, $\overline{V_{OS}}$	Common-Mode Offset Voltage	R_L = 100Ω			2.5	3	V
$\lvert V_T \rvert - \lvert \overline{V_T} \rvert$	Difference in Differential Output Voltage	R_L = 100Ω			0.05	0.4	V
$\lvert V_{OS} \rvert - \lvert \overline{V_{OS}} \rvert$	Difference in Common-Mode Offset Voltage	R_L = 100Ω			0.05	0.4	V
V_{SS}	$\lvert V_T - \overline{V_T} \rvert$	R_L = 100Ω, V_{CC} ≥ 4.75V		4.0	4.8		V
V_{CMR}	Output Voltage Common-Mode Range	$V_{DISABLE}$ = 2.4V		±10			V
I_{XA}	Output Leakage Current	V_{CC} = 0V	V_{CMR} = 10V			100	µA
I_{XB}	Power OFF		V_{CMR} = −10V			−100	µA
I_{OX}	TRI-STATE Output Current	V_{CC} = Max, V_{EE} = 0V and −5V	V_{CMR} ≤ 10V			100	µA
			V_{CMR} ≥ −10V			−100	µA
I_{SA}	Output Short Circuit Current	V_{IN} = 0.4V	V_{OA} = 6V		80	150	mA
			V_{OB} = 0V		−80	−150	mA
I_{SB}	Output Short Circuit Current	V_{IN} = 2.4V	V_{OA} = 0V		−80	−150	mA
			V_{OB} = 6V		80	150	mA
I_{CC}	Supply Current				18	30	mA

(1) Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS1691A and across the 0°C to +70°C range for the DS3691. All typicals are given for V_{CC} = 5V and T_A = 25°C. V_{CC} and V_{EE} as listed in operating conditions.
(2) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.
(3) Only one output at a time should be shorted.
(4) Symbols and definitions correspond to EIA RS-422 and/or RS-423 where applicable.

AC Electrical Characteristics[1]

T_A = 25°C

Parameter		Test Conditions	Min	Typ	Max	Units
RS-422 CONNECTION, V_{CC} = 5V, MODE SELECT = 0.8V						
t_r	Output Rise Time	R_L = 100Ω, C_L = 500 pF Figure 3		120	200	ns
t_f	Output Fall Time	R_L = 100Ω, C_L = 500 pF Figure 3		120	200	ns
t_{PDH}	Output Propagation Delay	R_L = 100Ω, C_L = 500 pF Figure 3		120	200	ns
t_{PDL}	Output Propagation Delay	R_L = 100Ω, C_L = 500 pF Figure 3		120	200	ns
t_{PZL}	TRI-STATE Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 pF Figure 6		250	350	ns
t_{PZH}	TRI-STATE Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 pF Figure 6		180	300	ns
t_{PLZ}	TRI-STATE Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 pF Figure 6		180	300	ns
t_{PHZ}	TRI-STATE Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 pF Figure 6		250	350	ns

(1) Symbols and definitions correspond to EIA RS-422 and/or RS-423 where applicable.

DC Electrical Characteristics(1)(2)(3)(4)

Parameter		Test Conditions		Min	Typ	Max	Units
RS-423 CONNECTION, $\|V_{CC}\| = \|V_{EE}\|$, MODE SELECT ≥ 2V							
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
I_{IH}	High Level Input Current	V_{IN} = 2.4V			1	40	µA
		V_{IN} ≤ 15V			10	100	µA
I_{IL}	Low Level Input Current	V_{IN} = 0.4V			−30	−200	µA
V_I	Input Clamp Voltage	I_{IN} = −12 mA				−1.5	V
V_O	Output Voltage	R_L = ∞, See(5) V_{CC} ≥ 4.75V	V_{IN} = 2V	4.0	4.4	6.0	V
$\overline{V_O}$			V_{IN} = 0.4V	−4.0	−4.4	−6.0	V
V_T	Output Voltage	R_L = 450Ω V_{CC} ≥ 4.75V	V_{IN} = 2.4V	3.6	4.1		V
$\overline{V_T}$			V_{IN} = 0.4V	−3.6	−4.1		V
$\|V_T\| - \|\overline{V_T}\|$	Output Unbalance	$\|V_{CC}\| = \|V_{EE}\|$ = 4.75V, R_L = 450Ω			0.02	0.4	V
I_X^+	Output Leakage Power OFF	$V_{CC} = V_{EE}$ = 0V	V_O = 6V		2	100	µA
I_X^-	Output Leakage Power OFF	$V_{CC} = V_{EE}$ = 0V	V_O = −6V		−2	−100	µA
I_S^+	Output Short Circuit Current	V_O = 0V	V_{IN} = 2.4V		−80	−150	mA
I_S^-	Output Short Circuit Current	V_O = 0V	V_{IN} = 0.4V		80	150	mA
I_{SLEW}	Slew Control Current				±140		µA
I_{CC}	Positive Supply Current	V_{IN} = 0.4V, R_L = ∞			18	30	mA
I_{EE}	Negative Supply Current	V_{IN} = 0.4V, R_L = ∞			−10	−22	mA

(1) Unless otherwise specified, min/max limits apply across the −55°C to +125°C temperature range for the DS1691A and across the 0°C to +70°C range for the DS3691. All typicals are given for V_{CC} = 5V and T_A = 25°C. V_{CC} and V_{EE} as listed in operating conditions.
(2) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.
(3) Only one output at a time should be shorted.
(4) Symbols and definitions correspond to EIA RS-422 and/or RS-423 where applicable.
(5) At −55°C, the output voltage is +3.9V minimum and −3.9V minimum.

AC Electrical Characteristics(1)

T_A = 25°C

Parameter		Test Conditions	Min	Typ	Max	Units
RS-423 CONNECTION, V_{CC} = 5V, V_{EE} −5V, MODE SELECT = 2.4V						
t_r	Rise Time	R_L = 450Ω, C_L = 500 pF, C_C = 0 Figure 4		120	300	ns
t_f	Fall Time	R_L = 450Ω, C_L = 500 pF, C_C = 0 Figure 4		120	300	ns
t_r	Rise Time	R_L = 450Ω, C_L = 500 pF C_C = 50 pF Figure 5		3.0		µs
t_f	Fall Time	R_L = 450Ω, C_L = 500 pF C_C = 50 pF Figure 5		3.0		µs
t_{rc}	Rise Time Coefficient	R_L = 450Ω, C_L = 500 pF, C_C = 50 pF Figure 5		0.06		µs/pF
t_{PDH}	Output Propagation Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 Figure 4		180	300	ns
t_{PDL}	Output Propagation Delay	R_L = 450Ω, C_L = 500 pF, C_C = 0 Figure 4		180	300	ns

(1) Symbols and definitions correspond to EIA RS-422 and/or RS-423 where applicable.

AC Test Circuits and Switching Time Waveforms

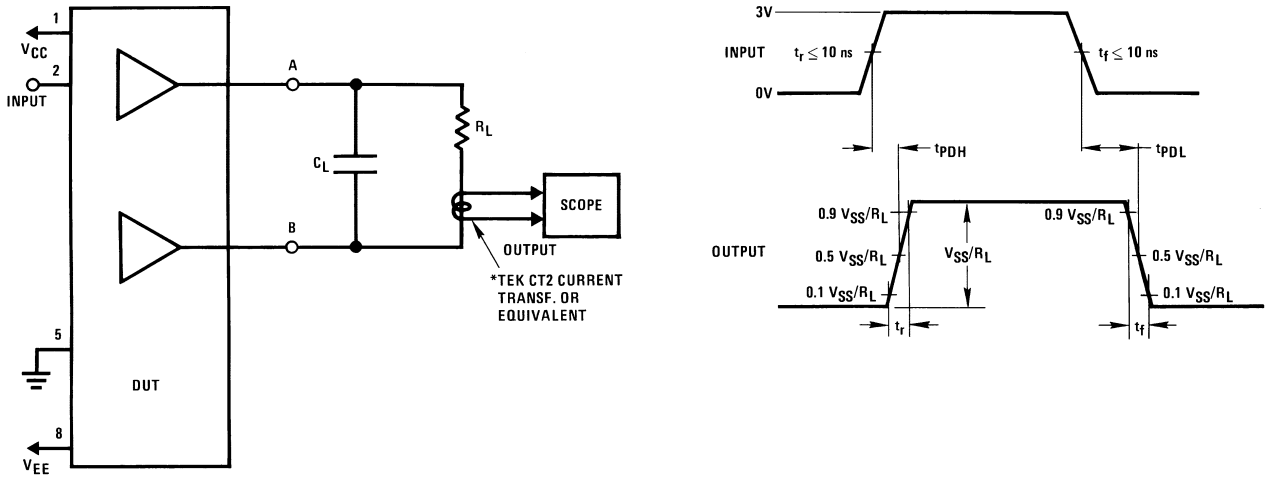


Figure 3. Differential Connection

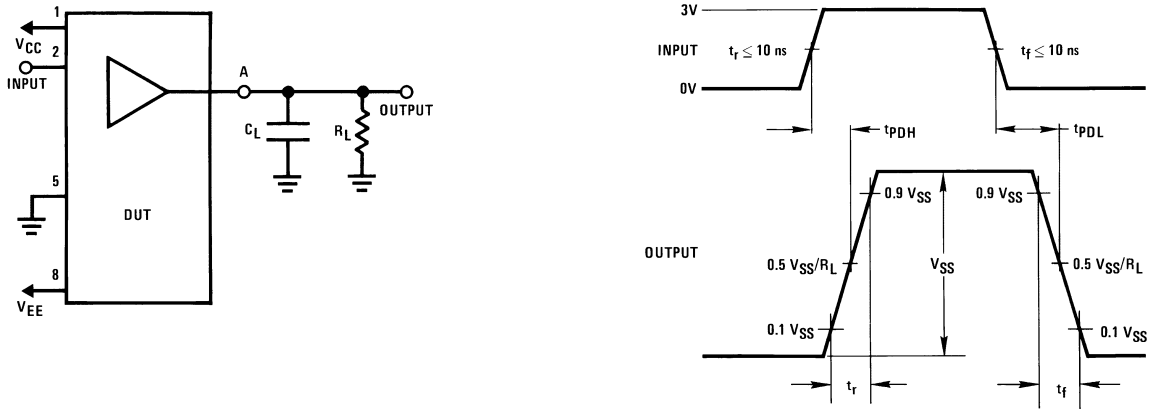
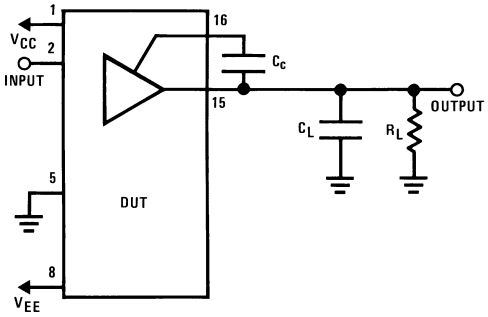


Figure 4. RS-423 Connection



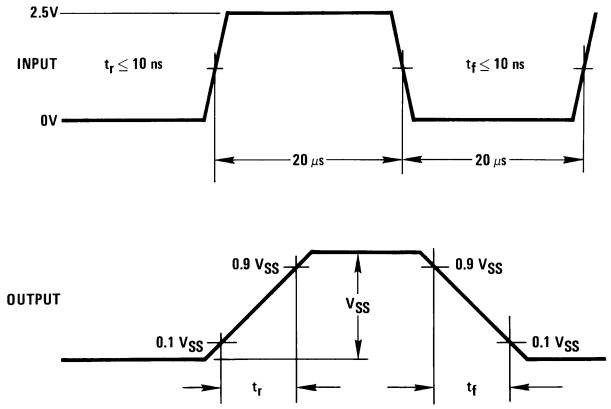


Figure 5. Rise Time Control for RS-423

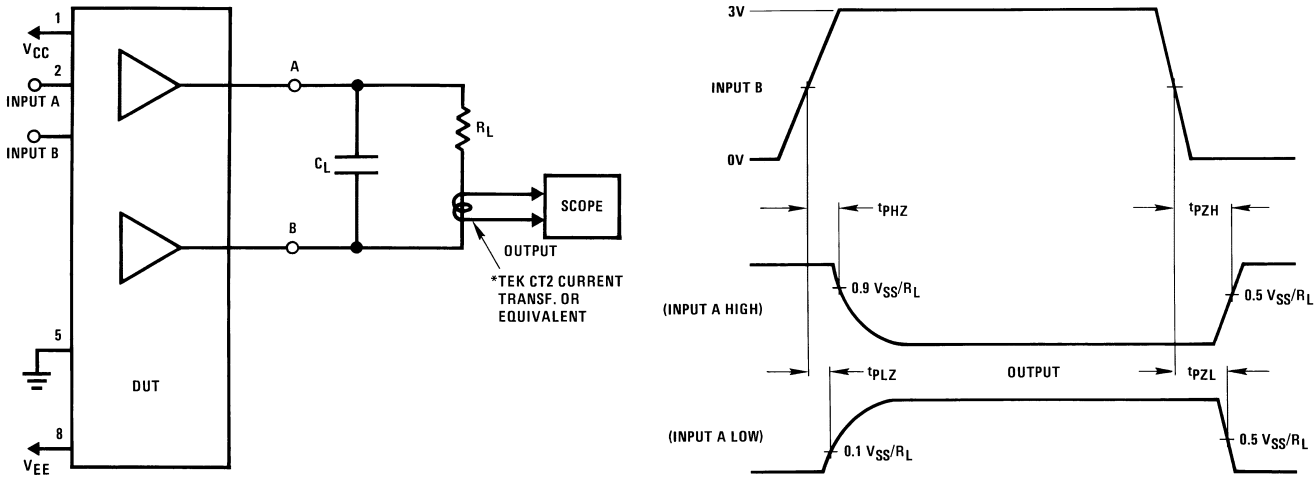


Figure 6. TRI-STATE Delays

SWITCHING WAVEFORMS

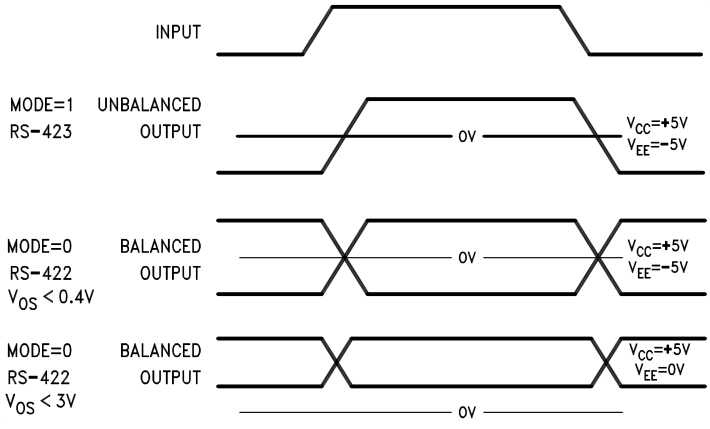


Figure 7. Typical Output Voltage

Truth Table

Operation	Inputs			Outputs	
	Mode	A (D)	B (C)	A (D)	B (C)
RS-422	0	0	0	0	1
	0	0	1	TRI-STATE	TRI-STATE
	0	1	0	1	0
	0	1	1	TRI-STATE	TRI-STATE
RS-423	1	0	0	0	0
	1	0	1	0	1
	1	1	0	1	0
	1	1	1	1	1

TYPICAL APPLICATION INFORMATION

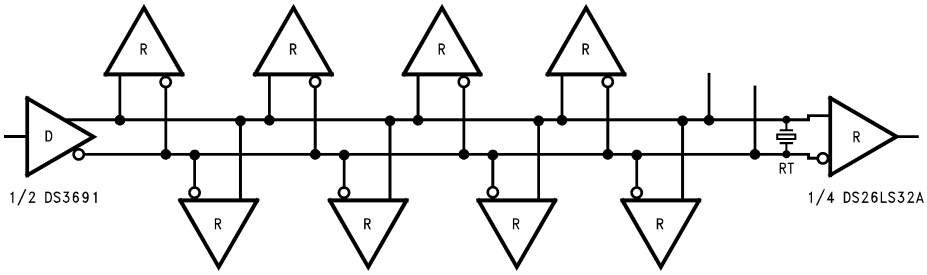


Figure 8. Fully Loaded RS-422 Interface

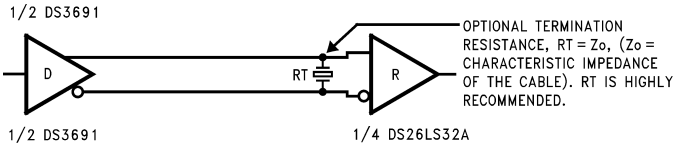


Figure 9. RS-422 Point to Point Application

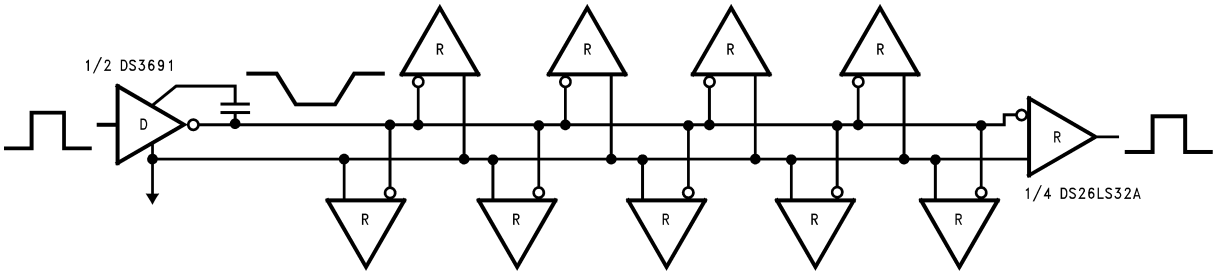
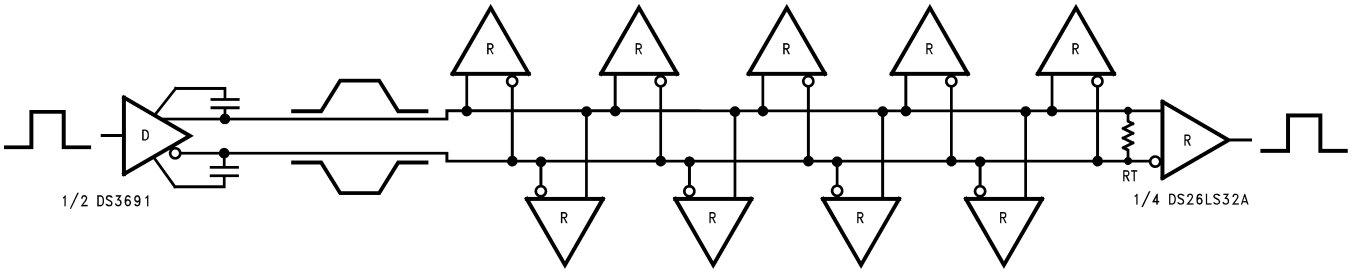


Figure 10. Fully Loaded RS-423 Interface



***Note:** Controlled edge allows longer stub lengths. Multiple Drivers are NOT allowed.

Figure 11. Differential Application with Rise Time Control

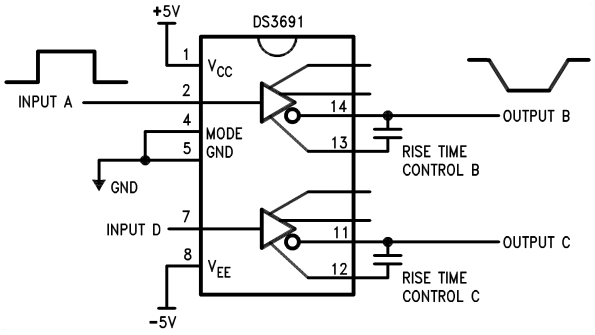


Figure 12. Dual RS-423 Inverting Driver

Typical Rise Time Control Characteristics

(RS-423 Mode)

Rise Time vs External Capacitor

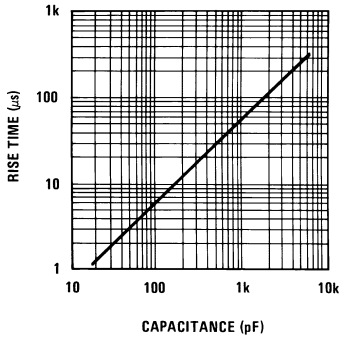


Figure 13.

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS3691M/NOPB	ACTIVE	SOIC	D	16	48	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS3691M AM26LS30SC	Samples
DS3691MX/NOPB	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	DS3691M AM26LS30SC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

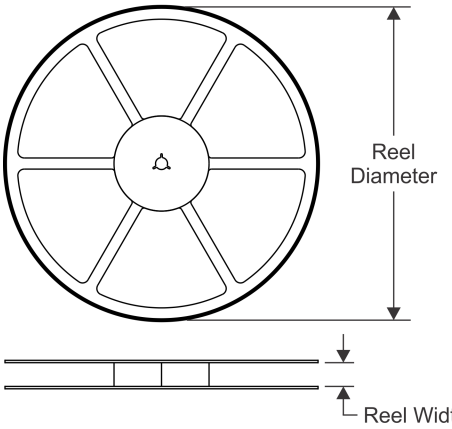
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

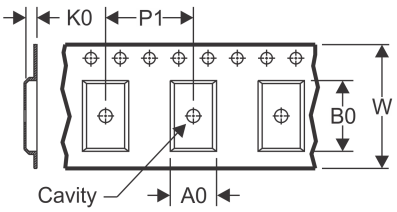
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

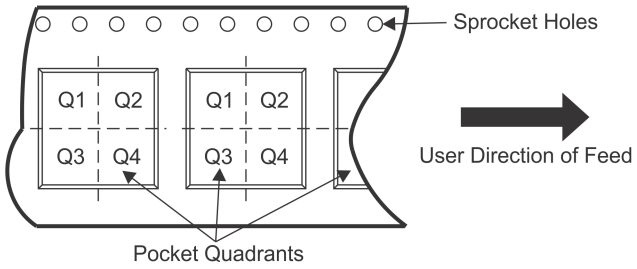


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

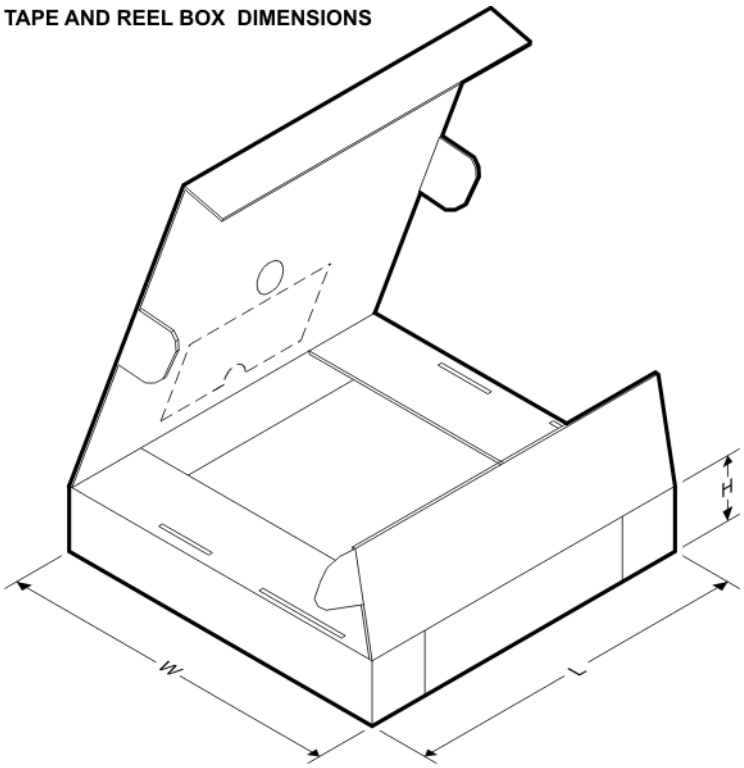
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS3691MX/NOPB	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.3	8.0	16.0	Q1

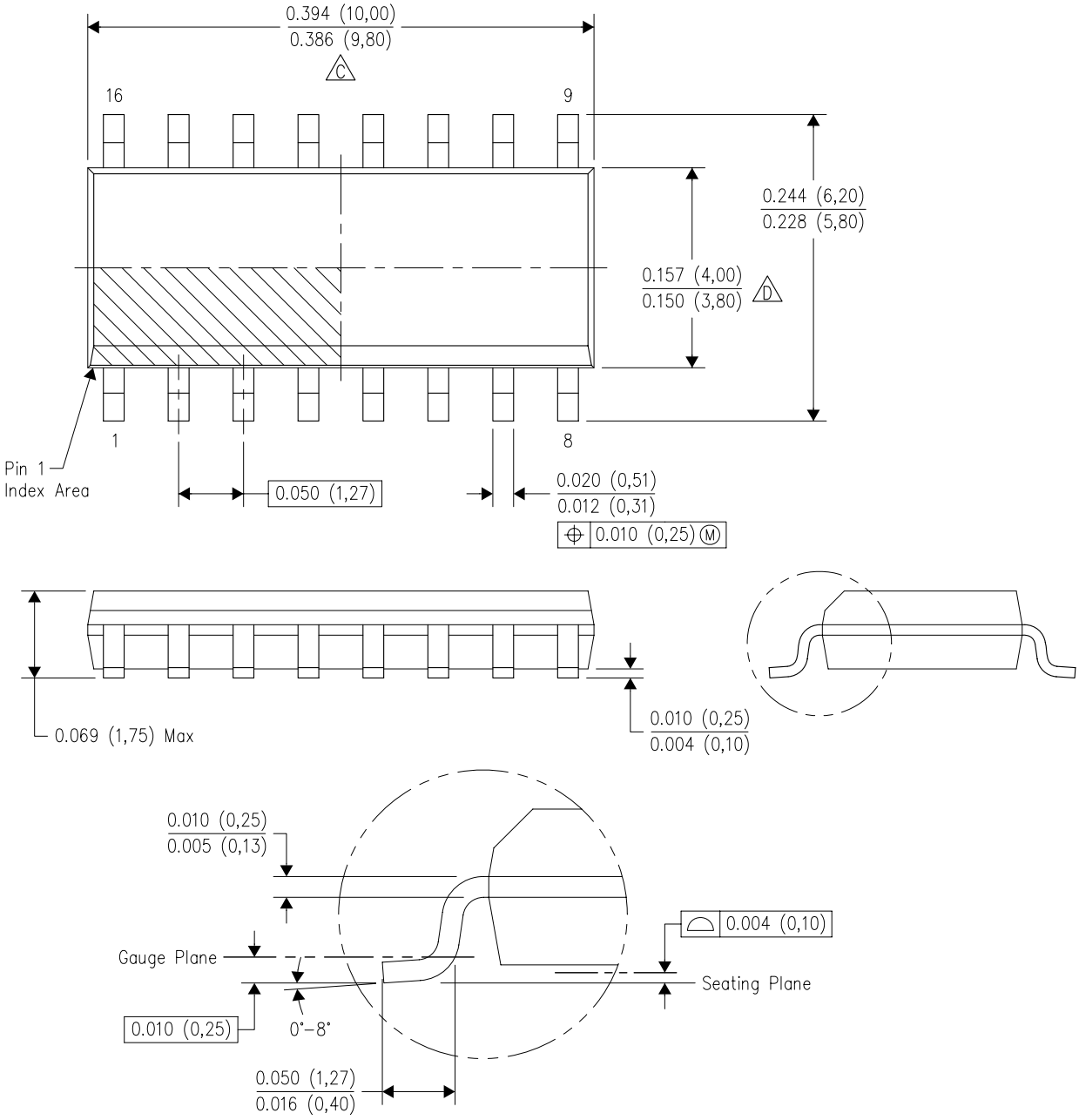
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS3691MX/NOPB	SOIC	D	16	2500	367.0	367.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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