



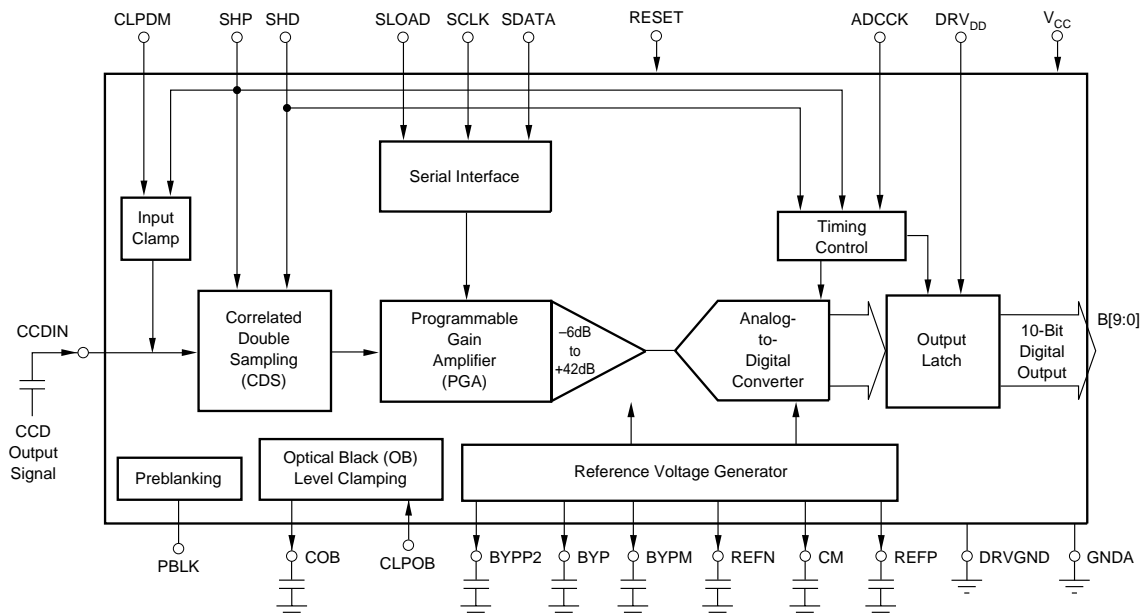
CCD SIGNAL PROCESSOR for DIGITAL CAMERAS

FEATURES

- **CCD SIGNAL PROCESSING:**
Correlated Double Sampling (CDS)
Programmable Black Level Clamping
- **PROGRAMMABLE GAIN AMPLIFIER (PGA):**
-6dB to +42dB Gain Ranging
- **10-BIT DIGITAL DATA OUTPUT:**
Up to 20MHz Conversion Rate
No Missing Codes
- **79dB SIGNAL-TO-NOISE RATIO**
- **PORTABLE OPERATION:**
Low Voltage: 2.7V to 3.6V
Low Power: 83mW (typ) at 3.0V
Stand-By Mode: 6mW

DESCRIPTION

The VSP2260 is a complete mixed-signal processing IC for digital cameras, providing signal conditioning and Analog-to-Digital (A/D) conversion for the output of a CCD array. The primary CCD channel provides Correlated Double Sampling (CDS) to extract video information from the pixels, -6dB to +42dB gain range with digital control for varying illumination conditions, and black level clamping for an accurate black level reference. Input signal clamping and offset correction of the input CDS are also performed. The stable gain control is linear in dB. Additionally, the black level is quickly recovered after gain change. The VSP2260Y is available in an LQFP-48 package and operates from a single +3V/+3.3V supply.



SPECIFICATIONS

At $T_A = +25^\circ\text{C}$, $V_{CC} = +3.0\text{V}$, $\text{DRV}_{DD} = +3.0\text{V}$, Conversion Rate (f_{ADCCK}) = 20MHz, unless otherwise noted.

PARAMETER	CONDITIONS	VSP2260Y			UNITS
		MIN	TYP	MAX	
RESOLUTION			10		Bits
CONVERSION RATE		20			MHz
DIGITAL INPUT Logic Family Input Voltage Input Current	LOW to HIGH Threshold Voltage (V_{T+}) HIGH to LOW Threshold Voltage (V_{T-}) Logic HIGH (I_{IH}) $V_{IN} = +3\text{V}$ Logic LOW (I_{IL}) $V_{IN} = 0\text{V}$		TTL 1.7 1.0		V V μA μA
DIGITAL OUTPUT Logic Family Logic Coding Output Voltage ADCCK Clock Duty Cycle Input Capacitance Maximum Input Voltage	Logic HIGH (V_{OH}) $I_{OH} = -2\text{mA}$ Logic LOW (V_{OL}) $I_{OL} = 2\text{mA}$	2.4	CMOS Straight Binary 50 5	0.4	V V % pF V
ANALOG INPUT (CCDIN) Input Signal Level for Full-Scale Out Input Capacitance Input Limit	PGA Gain = 0dB	900 -0.3	15	3.3	mV pF V
TRANSFER CHARACTERISTICS Differential Non-Linearity (DNL) Integral Non-Linearity (INL) No Missing Codes Step Response Settling Time Overload Recovery Time Data Latency Signal-to-Noise Ratio ⁽¹⁾ CCD Offset Correction Range	PGA Gain = 0dB PGA Gain = 0dB Full-Scale Step Input Step Input from 1.8V to 0V Grounded Input Cap, PGA Gain = 0dB Grounded Input Cap, Gain = +24dB	-180	± 0.5 ± 1 Guaranteed 1 2 9 (Fixed) 79 55	200	LSB LSB Pixel Pixels Clock Cycles dB dB mV
CDS Reference Sample Settling Time Data Sample Settling Time	Within 1LSB, Driver Impedance = 50 Ω Within 1LSB, Driver Impedance = 50 Ω			11 11	ns ns
INPUT CLAMP Clamp-On Resistance Clamp Level			400 1.5		Ω V
PROGRAMMABLE GAIN AMP (PGA) Gain-Control Resolution Maximum Gain High Gain Medium Gain Low Gain Minimum Gain Gain Control Error	Gain Code = 1111111111 Gain Code = 1101001000 Gain Code = 1000100000 Gain Code = 0010000000 Gain Code = 0000000000		10 42 34 20 0 -6 ± 0.5		Bits dB dB dB dB dB dB
OPTICAL BLACK CLAMP LOOP Control DAC Resolution Optical Black Clamp Level Min Output Current for Control DAC Max Output Current for Control DAC Loop Time Constant Slew Rate	Programmable Range of Clamp Level OBCLP Level at CODE = 1000 COB Pin COB Pin $C_{\text{COB}} = 0.1\mu\text{F}$ $C_{\text{COB}} = 0.1\mu\text{F}$, Output Current from Control DAC is Saturated	0	10 32 ± 0.15 ± 153 40.7 1530	60	Bits LSB LSB μA μA μs V/s
REFERENCE Positive Reference Voltage Negative Reference Voltage			1.75 1.25		V V
POWER SUPPLY Supply Voltage Power Dissipation	V_{CC} , DRV_{DD} Normal Operation Mode: No Load, DAC0 and DAC1 are Suspended Stand-By Mode: $f_{\text{ADCCK}} = \text{Not Apply}$	2.7	3.0 83 6	3.6	V mW mW
TEMPERATURE RANGE Operating Temperature Thermal Resistance	θ_{JA} LQFP-48	-25	100	+85	$^\circ\text{C}$ $^\circ\text{C/W}$

NOTE: (1) SNR = 20 log(full-scale voltage/rms noise).

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage: V_{CC} , DRV_{DD}	+4.0V
Supply-Voltage Differences: Among V_{CC}	$\pm 0.1V$
Ground-Voltage Differences: Among GNDs	$\pm 0.1V$
Digital Input Voltage	-0.3 to +5.3V
Analog Input Voltage	-0.3 to $V_{CC} + 0.3V$
Input Current (Any Pins Except Supplies)	$\pm 10mA$
Ambient Temperature Under Bias	-40 to +125°C
Storage Temperature	-55 to +125°C
Junction Temperature	+150°C
Lead Temperature (Soldering, 5s)	+260°C
Package Temperature (IR Reflow, Peak, 10s)	+235°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

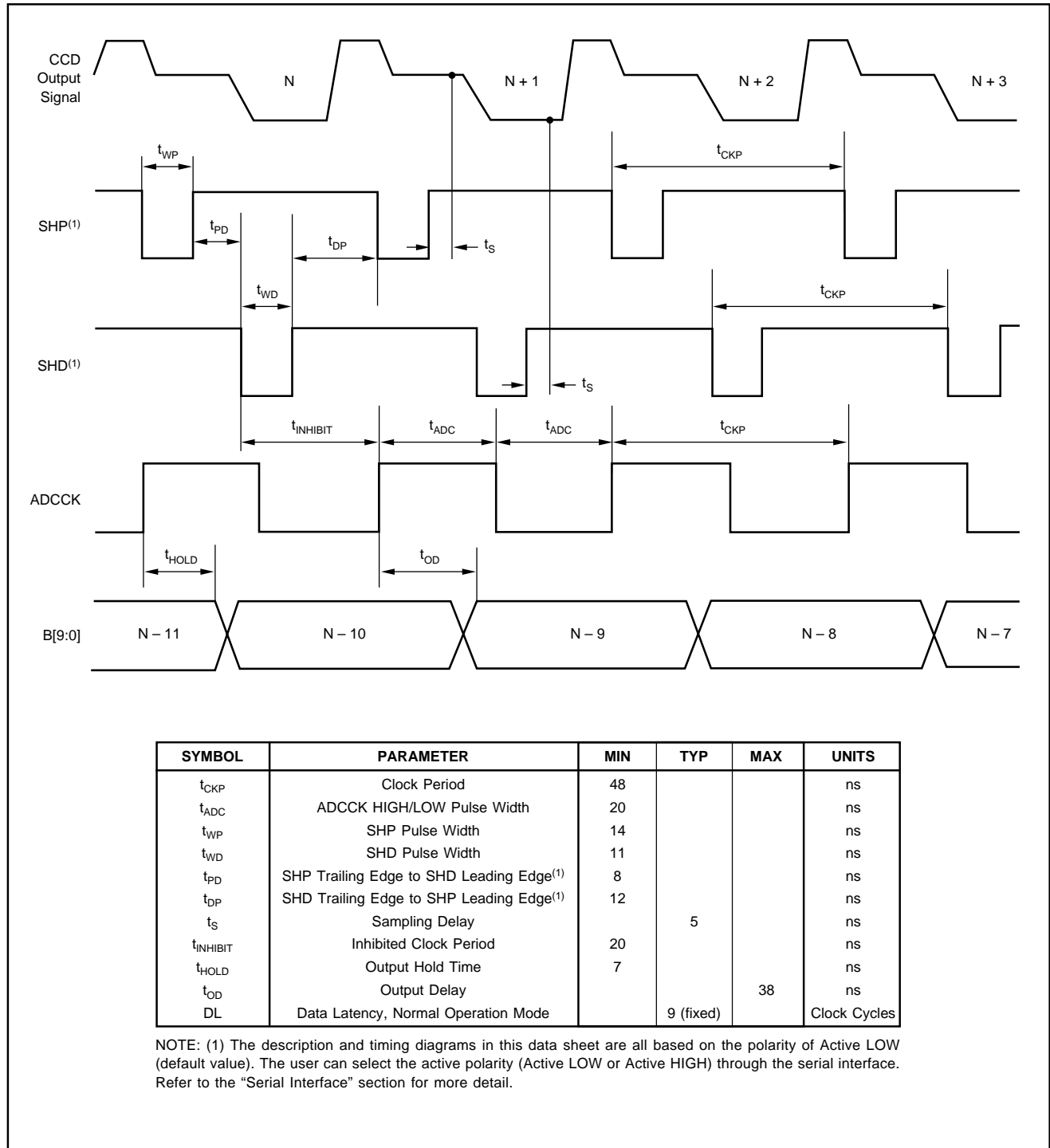
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER ⁽¹⁾	TRANSPORT MEDIA
VSP2260Y "	LQFP-48 "	340 "	0 to +85°C "	VSP2260Y "	VSP2260Y VSP2260Y/2K	250-Piece Tray Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K indicates 2000 devices per reel). Ordering 2000 pieces of "VSP2260Y/2K" will get a single 2000 piece Tape and Reel.

DEMO BOARD ORDERING INFORMATION

PRODUCT	ORDERING NUMBER
VSP2260Y	DEM-VSP2260Y

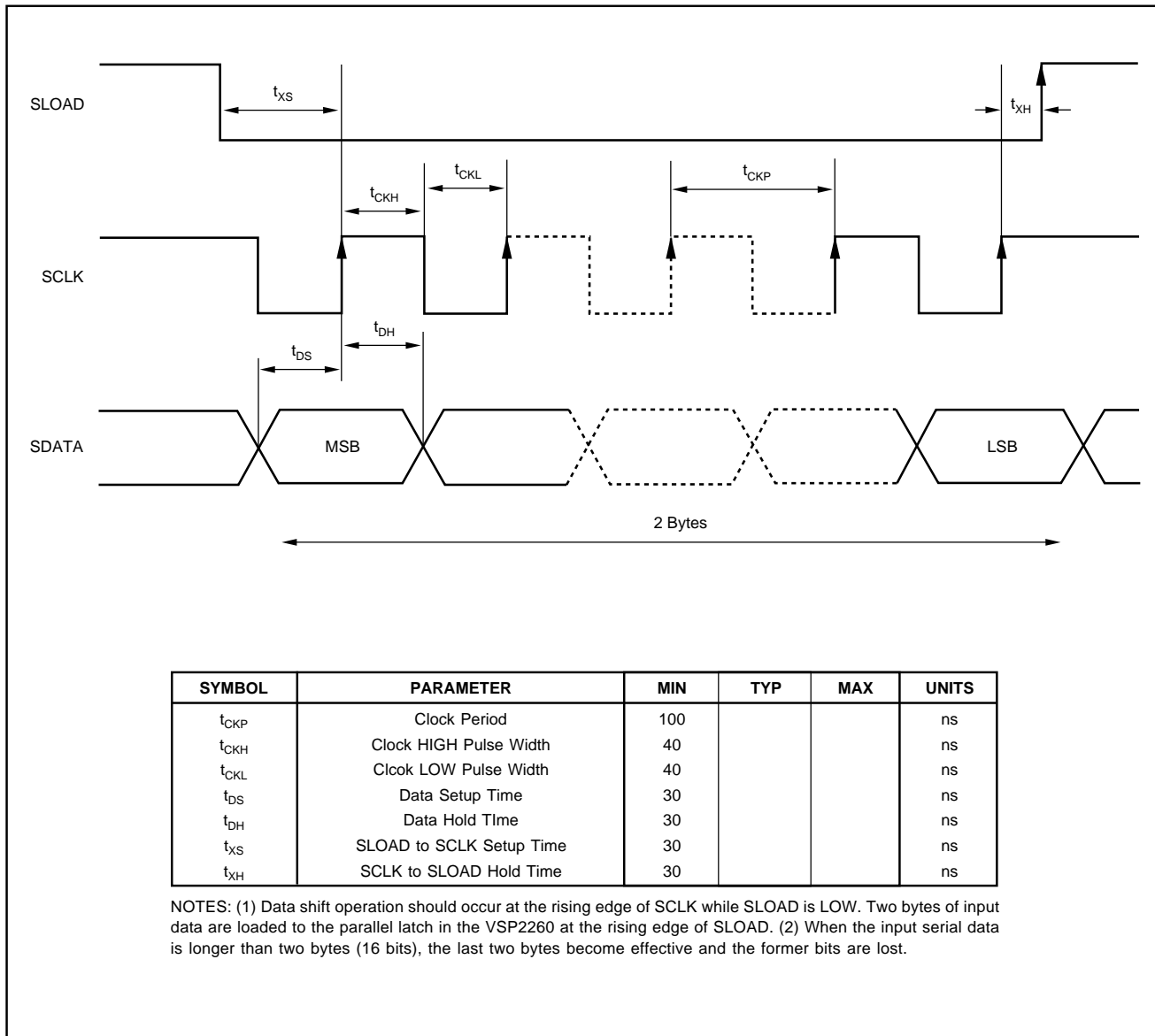
CDS TIMING SPECIFICATIONS



SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{CKP}	Clock Period	48			ns
t_{ADC}	ADCCK HIGH/LOW Pulse Width	20			ns
t_{WP}	SHP Pulse Width	14			ns
t_{WD}	SHD Pulse Width	11			ns
t_{PD}	SHP Trailing Edge to SHD Leading Edge ⁽¹⁾	8			ns
t_{DP}	SHD Trailing Edge to SHP Leading Edge ⁽¹⁾	12			ns
t_S	Sampling Delay		5		ns
$t_{INHIBIT}$	Inhibited Clock Period	20			ns
t_{HOLD}	Output Hold Time	7			ns
t_{OD}	Output Delay			38	ns
DL	Data Latency, Normal Operation Mode		9 (fixed)		Clock Cycles

NOTE: (1) The description and timing diagrams in this data sheet are all based on the polarity of Active LOW (default value). The user can select the active polarity (Active LOW or Active HIGH) through the serial interface. Refer to the "Serial Interface" section for more detail.

SERIAL INTERFACE TIMING SPECIFICATIONS



THEORY OF OPERATION

INTRODUCTION

The VSP2260 is a complete mixed-signal IC that contains all of the key features associated with the processing of the CCD imager output signal in a video camera, a digital still camera, security camera, or similar applications (see the simplified block diagram on page 1 for details). The VSP2260 includes a Correlated Double Sampler (CDS), Programmable Gain Amplifier (PGA), Analog-to-Digital Converter (ADC), input clamp, Optical Black (OB) level clamp loop, serial interface, timing control, and reference voltage generator. We recommend an off-chip emitter follower buffer between the CCD output and the VSP2260 CCDIN input. The PGA gain control, clock polarity setting, and operation mode can be selected through the serial interface. All parameters are reset to the default value when the RESET pin goes LOW asynchronously from the clocks.

CORRELATED DOUBLE SAMPLER (CDS)

The output signal of a CCD imager is sampled twice during one pixel period: once at the reference interval and the other at the data interval. Subtracting these two samples from each other extracts the video information of the pixel as well as removes any noise that is common, or correlated, to both the intervals. Thus, the CDS is very important in reducing the reset noise and low-frequency noises that are present on the CCD output signal. Figure 1 shows the simplified block diagram of the CDS and input clamp.

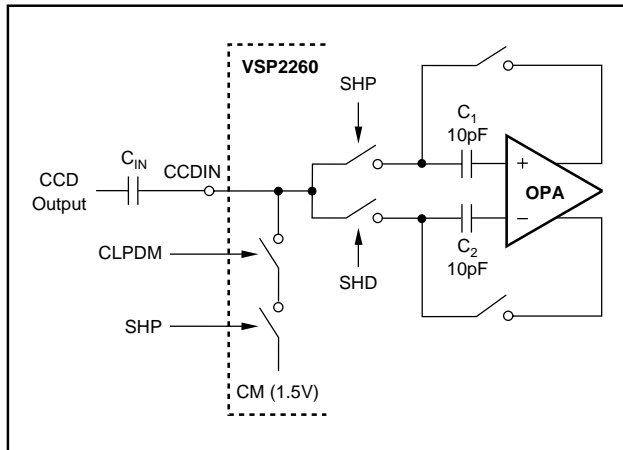


FIGURE 1. Simplified Block Diagram of CDS and Input Clamp.

The CDS is driven through an off-chip coupling capacitor (C_{IN}). AC coupling is strongly recommended because the DC level of the CCD output signal is usually several volts too high for the CDS to work properly.

A $0.1\mu\text{F}$ capacitor is recommended for C_{IN} , depending on the application environment. Additionally, we recommend an off-chip emitter follower buffer that can drive more than 10pF , because the 10pF capacitor and a few pF of stray capacitance can be seen at the input pin. The analog input

signal range at the CCDIN pin is $1\text{V}_{\text{p-p}}$, and the appropriate common-mode voltage for the CDS is around 0.5V to 1.5V .

The reference level is sampled during SHP active period, and the voltage level is held on sampling capacitor C_1 at the trailing edge of SHP. The data level is sampled during SHD active period, and the voltage level is held on the sampling capacitor C_2 at the trailing edge of SHD. The switched-capacitor amplifier then performs the subtraction of these two levels.

The user can select the active polarity of SHP/SHD (Active HIGH or Active LOW) through the serial interface (refer to the “Serial Interface” section for more detail). The default value of SHP/SHD is “Active LOW”. However, immediately after power ON, this value is Unknown. For this reason, the appropriate value must be set by using the serial interface, or reset to the default value by strobing the RESET pin. The descriptions and the timing diagrams in this data sheet are all based on the polarity of Active LOW (default value).

INPUT CLAMP OR DUMMY PIXEL CLAMP

The buffered CCD output is capacitively coupled to the VSP2260. The purpose of the input clamp is to restore the DC component of the input signal that was lost with the AC coupling and establish the desired DC bias point for the CDS. A simplified block diagram of the input clamp is shown in Figure 1. The input level is clamped to the internal reference voltage, CM (1.5V), during the dummy pixel interval. More specifically, when both CLPDM and SHP are active, the dummy clamp function becomes active. If the dummy pixels and/or the CLPDM pulse are not available in your system, the CLPOB pulse can be used in place of CLPDM, as long as the clamping takes place during black pixels. In this case, both the CPLDM pin (active at same timing as CLPOB) and SHP become active during the optical black pixel interval, and then the dummy clamp function becomes active.

The active polarity of CLPDM and SHP (Active HIGH or Active LOW) can be selected through the serial interface (refer to the “Serial Interface” section for more detail). The default value of CLPDM and SHP is “Active LOW”. However, immediately after power ON, this value is Unknown. For this reason, the appropriate value must be set by using the serial interface, or reset to the default value by strobing the RESET pin. The descriptions and the timing diagrams in this data sheet are all based on the polarity of Active LOW (default value).

HIGH PERFORMANCE ANALOG-TO-DIGITAL CONVERTER (ADC)

The ADC utilizes a fully differential and pipelined architecture. This ADC is well suited for low-voltage operations, low power consumption requirements, and high-speed applications. It guarantees 10-bit resolution with no missing codes. The VSP2260 includes a reference voltage generator for the ADC. REFP (Positive Reference, pin 38), REFN

(Negative Reference, pin 39), and CM (Common-Mode Voltage, pin 37) should be bypassed to ground with a 0.1µF ceramic capacitor and should not be used elsewhere in the system, as they affect the stability of these reference levels, which causes ADC performance degradation. Note that these are analog output pins and, therefore, do not apply external voltage.

PROGRAMMABLE GAIN AMPLIFIER (PGA)

Figure 2 shows the characteristics of the PGA gain. The PGA provides a gain range of -6dB to +42dB, which is linear in dB. The gain is controlled by a digital code with 10-bit resolution, and can be set through the serial interface (refer to the “Serial Interface” section for more detail). The default value of the gain control code is 128 (PGA Gain = 0dB). However, immediately after power ON, this value is Unknown. For this reason, the appropriate value must be set by using the serial interface, or reset to the default value by strobing the RESET pin.

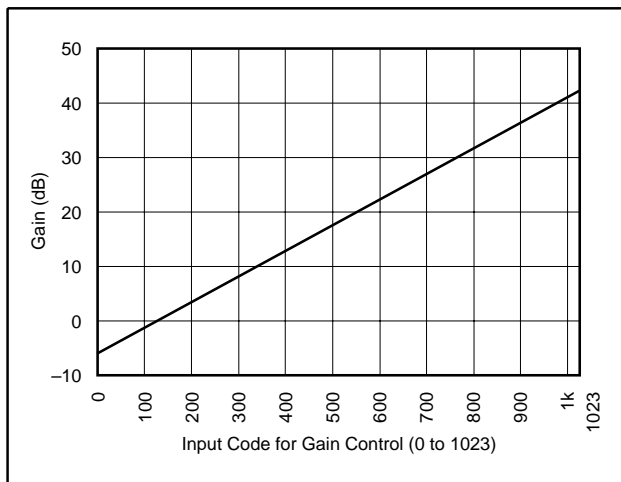


FIGURE 2. The Characteristics of PGA Gain.

OPTICAL BLACK (OB) LEVEL CLAMP LOOP

To extract the video information correctly, the CCD signal must be referenced to a well-established OB level. The VSP2260 has an auto-calibration loop to establish the OB level using the optical black pixels output from the CCD imager. The input signal level of the OB pixels is identified as the real “OB level”, and the loop should be closed while CLPOB is active.

During the effective pixel interval, the reference level of the CCD output signal is clamped to the OB level by the OB level clamp loop. To determine the loop time constant, an off-chip capacitor is required, and should be connected to COB (pin 28). Time constant T is given in the following equation:

$$T = C / (16384 \cdot I_{MIN})$$

Where C is the capacitor value connected to COB, I_{MIN} is the minimum current (0.15µA) of the control Digital-to-Analog Converter (DAC) in the OB level clamp loop, and 0.15µA is

equivalent to 1LSB of the DAC output current. When C is 0.1µF, time constant T is 40.7µs.

Additionally, the slew rate SR is given the following equation:

$$SR = I_{MAX} / C$$

Where C is the capacitor value connected to COB, I_{MAX} is the maximum current (153µA) of the control DAC in the OB level clamp loop, and 153µA is equivalent to 1023LSB of the DAC output current.

Generally, OB level clamping at high speed causes “Clamp Noise” (or “White Streak Noise”), however, the noise will decrease by increasing C. On the other hand, an increased C requires a much longer time to restore from Stand-By mode, or right after power ON. Therefore, we consider 0.1µF to 0.22µF a reasonable value for C. However, it depends on the application environment; we recommend making careful adjustments using trial-and-error.

The “OB clamp level” (the pedestal level) is programmable through the serial interface (refer to the “Serial Interface” section for more detail). Table I shows the relationship between input code and the OB clamp level.

INPUT CODE	OB CLAMP LEVEL, LSBs OF 10 BITS
0000	0LSB
0001	4LSB
0010	8LSB
0011	12LSB
0100	16LSB
0101	20LSB
0110	24LSB
0111	28LSB
1000 (Default)	32LSB
1001	36LSB
1010	40LSB
1011	44LSB
1100	48LSB
1101	52LSB
1110	56LSB
1111	60LSB

TABLE I. Programmable OB Clamp Level.

The active polarity of CLPOB (Active HIGH or Active LOW) can be selected through the serial interface (refer to the “Serial Interface” section for more detail). The default value of CLPOB is “Active LOW”. However, immediately after power ON, this value is Unknown. For this reason, the appropriate value must be set by using the serial interface, or reset to the default value by strobing the RESET pin. The descriptions and the timing diagrams in this data sheet are all based on the polarity of Active LOW (default value).

PREBLANKING AND DATA LATENCY

The VSP2260 has an input blanking, or preblanking, function. When PBLK goes LOW, all digital outputs will go to ZERO at the 11th rising edge of ADCK. In this mode, the digital output data comes out on the rising edge of ADCK with a delay of 11 clock cycles (data latency is 11). This is different from the preblanking mode in which the digital

output data comes out on the rising edge of ADCK with a delay of nine clock cycles (data latency is nine).

If the input voltage is higher than the supply rail by 0.3V, or lower than the ground rail by 0.3V, the protection diodes will be turned on to prevent the input voltage from going any further. Such a high swing signal may cause device damage to the VSP2260 and should be avoided.

STAND-BY MODE

For the purpose of saving power, the VSP2260 can be set to Stand-by mode (or Power-Down mode) through the serial interface when the VSP2260 is not in use. Refer to the “Serial Interface” section for more detail. In this mode, all the function blocks are disabled and the digital outputs will go to all ZEROs, causing the current consumption to drop to 1mA. Since all the bypass capacitors will discharge during this mode, a substantial time (usually of the order of 200ms to 300ms) is required to power up from Stand-by mode.

VOLTAGE REFERENCE

All the reference voltages and bias currents needed in the VSP2260 are generated by its internal bandgap circuitry. The CDS and the ADC use mainly three reference voltages: REFP (Positive Reference, pin 38), REFN (Negative Reference, pin 39) and CM (Common-Mode Voltage, pin 37). REFP, REFN and CM should be heavily decoupled with appropriate capacitors (e.g., 0.1 μ F ceramic capacitor). Do not use these voltages elsewhere in the system as they affect the stability of the reference level, and cause ADC performance degradation. Note that these are analog output pins and do not apply external voltage.

BYPP2 (pin 29), BYP (pin 31), and BYPM (pin 32) are also reference voltages to be used in the analog circuit. BYP should be connected to ground with a 0.1 μ F ceramic capaci-

tor. Since the capacitor value for BYPP2 and BYPM affects the step response, we consider 400pF to 9000pF to be a reasonable value. However, as it depends on the application environment, we recommend making careful adjustments using trial-and-error.

BYPP2, BYP and BYPM should all be heavily decoupled with appropriate capacitors, and not used elsewhere in the system. They affect the stability of the reference levels, and cause performance degradation. Note that these are analog output pins and do not apply external voltage.

SERIAL INTERFACE

The serial interface has a 2-byte shift register and various parallel registers to control all the digitally programmable features of the VSP2260. Writing to these registers is controlled by four signals (SLOAD, SCLK, SDATA, and RESET). To enable the shift register, SLOAD must be pulled LOW. SDATA is the serial data input and the SCLK is the shift clock. The data at SDATA is taken into the shift register at the rising edge of SCLK; the data length should be two bytes. After the 2-byte shift operation, the data in the shift register is transferred to the parallel latch at the rising edge of SLOAD. In addition to the parallel latch, there are several registers dedicated to the specific features of the device and are synchronized with ADCK. It takes five or six clock cycles for the data in the parallel latch to be written to those registers. Therefore, to complete the data updates, it requires five or six clock cycles after parallel latching by the rising edge of SLOAD.

See Table II for the serial interface data format. TEST is the flag for the test mode (Texas Instruments proprietary only), A0 to A2 is the address for the various registers, and D0 to D11 is the data (or operand) field.

REGISTERS	MSB ← → LSB															
	TEST	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Configuration	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C0
PGA Gain	0	0	0	1	0	0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0
OB Clamp Level	0	0	1	0	0	0	0	0	0	0	0	0	O3	O2	O1	O0
Clock Polarity	0	0	1	1	0	0	0	0	0	0	0	0	0	P2	P1	P0
Reserved	0	1	0	0	x	x	x	x	x	x	x	x	x	x	x	x
Reserved	0	1	0	1	x	x	x	x	x	x	x	x	x	x	x	x
Reserved	0	1	1	0	x	x	x	x	x	x	x	x	x	x	x	x
Reserved	0	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x
Reserved	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x = Don't Care.

TABLE II. Serial Interface Data Format.

REGISTER DEFINITIONS

C[0] Operation Mode, Normal/Stand-By

Serial Interface and Registers are always active, independently from the operation mode.

C0 = Operation Mode for the entire chip except the serial interface and registers.

(C0 = 0 “Active”; C0 = 1 “Stand-by”)

G[9:0] The Characteristics of PGA Gain (refer to Figure 2)

O[3:0] Programmable OB Clamp Level (refer to Table I)

P[2:0] Clock Polarity

P0 = Polarity for CLPDM (P0 = 0 “Active LOW”; P0 = 1 “Active HIGH”)

P1 = for CLPOB (P0 = 0 “Active LOW”; P0 = 1 “Active HIGH”)

P2 = for SHP/SHD (P0 = 0 “Active LOW”; P0 = 1 “Active HIGH”)

Immediately after power ON, these values are Unknown. The appropriate value must be set by using the serial interface, or reset to the default value by strobing the RESET pin.

Default values are:

C[2:0] = 0 Normal Operation Mode

G[9:0] = 0010000000 PGA Gain = 0dB

O[3:0] = 1000 OB Clamp Level = 32LSB

P[2:0] = 000 CLPDM, CLPOB, SHP/SHD are all “Active LOW”⁽¹⁾

NOTE: (1) The descriptions and the timing diagrams in this data sheet are all based on the polarity of Active LOW (default value).

TIMINGS

The CDS and the ADC are operated by SHP/SHD and their derivative timing clocks generated by the on-chip timing generator. The digital output data is synchronized with ADCK. See the VSP2260 “CDS Timing Specifications” for the timing relationship among the CCD signal, SHP/SHD, ADCK and the output data. CLPOB is used to activate the black level clamp loop during the OB pixel interval, and CLPDM is used to activate the input clamping during the dummy pixel interval. If the CLPDM pulse is not available in your system, the CLPOB pulse can be used in place of CLPDM as long as the clamping takes place during black pixels (refer to the “Input Clamp and Dummy Pixel Clamp” section for more detail). The clock polarities of SHP/SHD, CLPOB and CLPDM can be independently set through the serial interface (refer to the “Serial Interface” section for more detail). The descriptions and the timing diagrams in this data sheet are all based on the polarity of Active LOW (default value). In order to keep a stable and accurate OB clamp level, we recommend CLPOB should not be activated during PBLK active period. Refer to the “Preblanking and Data Latency” section for more detail. In Stand-By mode, ADCK, SHP, SHD, CLPOB and CLPDM are internally masked and pulled HIGH.

POWER-SUPPLY, GROUNDING, AND DEVICE DECOUPLING RECOMMENDATIONS

The VSP2260 incorporates analog circuitry and a very high-precision, high-speed ADC that are vulnerable to any extraneous noise from the rails or elsewhere. For this reason, it should be treated as an analog component and all supply pins except for DRV_{DD} should be powered by the only analog supply of the system. This will ensure the most consistent results, since digital power lines often carry high levels of wideband noise that would otherwise be coupled into the device and degrade the achievable performance. Proper grounding, short lead length, and the use of ground

planes are also very important for high-frequency designs. Multi-layer PC boards are recommended for the best performance, since they offer distinct advantages like minimizing ground impedance, separation of signal layers by ground layers, etc. It is highly recommended that analog and digital ground pins of the VSP2260 be joined together at the IC and be connected only to the analog ground of the system. The driver stage of the digital outputs (B[9:0]) is supplied through a dedicated supply pin (DRV_{DD}) and it should be separated from the other supply pins completely, or at least with a ferrite bead.

It is also recommended to keep the capacitive loading on the output data lines as low as possible (typically less than 15pF). Larger capacitive loads demand higher charging current surges that can feed back into the analog portion of the VSP2260 and affect the performance. If possible, external buffers or latches should be used, providing the added benefit of isolating the VSP2260 from any digital noise activities on the data lines. In addition, resistors in series with each data line may help minimize the surge current. Values in the range of 100Ω to 200Ω will limit the instantaneous current the output stage has to provide for recharging the parasitic capacitances as the output levels change from LOW to HIGH, or HIGH to LOW. Due to high operation speed, the converter also generates high-frequency current transients and noises that are fed back into the supply and reference lines. This requires the supply and reference pins to be sufficiently bypassed. In most cases, 0.1μF ceramic chip capacitors are adequate to decouple the reference pins. Supply pins should be decoupled to the ground plane with a parallel combination of tantalum (1μF to 22μF) and ceramic (0.1μF) capacitors. The effectiveness of the decoupling largely depends on the proximity to the individual pin. DRV_{DD} should be decoupled to the proximity of $DRVGND$. Special attention must be paid to the bypassing of COB, BYPP2 and BYPM, since these capacitor values determine important analog performances of the device.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
VSP2260Y	ACTIVE	LQFP	PT	48	250	None	CU SNPB	Level-1-235C-UNLIM
VSP2260Y/2K	ACTIVE	LQFP	PT	48	2000	None	CU SNPB	Level-1-235C-UNLIM
VSP2260Y/2KC	ACTIVE	LQFP	PT	48	2000	None	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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