

## SNx4LVCH245A Octal Bus Transceivers With 3-State Outputs

### 1 Features

- Operate From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 6.3 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- $I_{off}$  Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Bus Hold on Data Inputs Eliminates the Need for External Pullup or Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

### 2 Applications

- Servers
- PCs and Notebooks
- Network Switches
- Wearable Health and Wellness Devices
- Telecom Infrastructures
- Electronic Points of Sale

### 3 Description

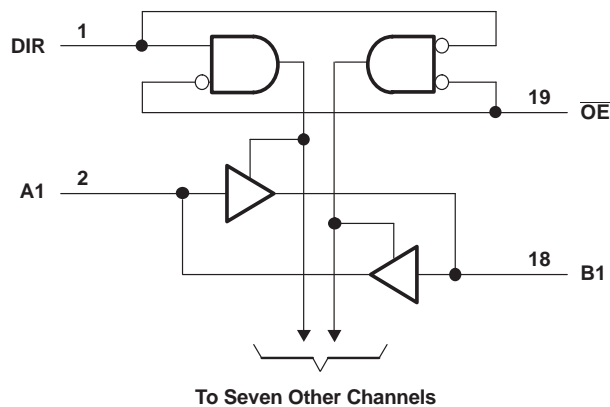
The SN54LVCH245A octal bus transceiver is designed for 2.7-V to 3.6-V  $V_{CC}$  operation, and the SN74LVCH245A octal bus transceiver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation. Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNx4LVCH245A	SSOP (20)	7.20 mm x 5.30 mm
	TVSOP (20)	5.00 mm x 4.40 mm
	SOIC (20)	12.80 mm x 7.50 mm
	SSOP (20)	12.60 mm x 5.30 mm
	TSSOP (20)	6.50 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### 4 Simplified Schematic



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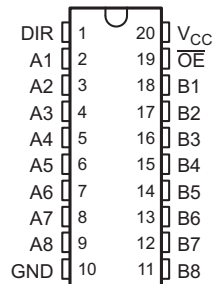
## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

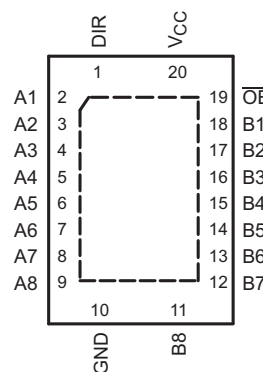
<b>Changes from Revision O (December 2005) to Revision P</b>	<b>Page</b>
• Updated document to new TI data sheet standards. ....	1
• Deleted Ordering Information table. ....	1
• Updated $I_{off}$ Feature bullet. ....	1
• Added Military Disclaimer to Features list. ....	1
• Added Applications. ....	1
• Added Device Information table. ....	1
• Added Handling Ratings table. ....	5
• Changed MAX operating temperature to 125°C. ....	6
• Added Thermal Information table. ....	6
• Added –40°C TO 125°C to Electrical Characteristics table .....	7
• Added data to –40°C TO 85°C Switching Characteristics table .....	8
• Added Switching Characteristics table for –40°C to 125°C for SN74LVCH245A. ....	8
• Added data to Operating Characteristics table. ....	8
• Added Typical Characteristics. ....	9
• Added Detailed Description section .....	11
• Added Application and Implementation section .....	12

## 6 Pin Configuration and Functions

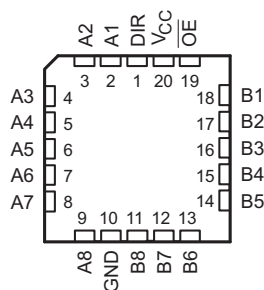
SN54LVCH245A . . . J OR W PACKAGE  
SN74LVCH245A . . . DB, DGV, DW, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74LVCH245A . . . RGY PACKAGE  
(TOP VIEW)



SN54LVCH245A . . . FK PACKAGE  
(TOP VIEW)



### Pin Functions

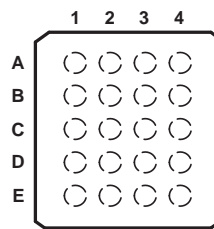
PIN		I/O	DESCRIPTION
NO.	NAME		
1	DIR	—	Direction pin
2	A1	I/O	A1 input or output
3	A2	I/O	A2 input or output
4	A3	I/O	A3 input or output
5	A4	I/O	A4 input or output
6	A5	I/O	A5 input or output
7	A6	I/O	A6 input or output
8	A7	I/O	A7 input or output
9	A8	I/O	A8 input or output
10	GND	—	Ground pin
11	Y8	I/O	Y8 input or output
12	Y7	I/O	Y7 input or output
13	Y6	I/O	Y6 input or output
14	Y5	I/O	Y5 input or output
15	Y4	I/O	Y4 input or output
16	Y3	I/O	Y3 input or output
17	Y2	I/O	Y2 input or output
18	Y1	I/O	Y1 input or output
19	$\overline{\text{OE}}$	I	Output enable
20	VCC	—	Power pin

**SN54LVCH245A, SN74LVCH245A**

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**GQN OR ZQN PACKAGE  
(TOP VIEW)**



**Table 1. Pin Assignments for GQN or ZQN Packages**

	<b>1</b>	<b>2</b>	<b>3</b>	<b>4</b>
<b>A</b>	A1	DIR	V <sub>CC</sub>	$\overline{OE}$
<b>B</b>	A3	B2	A2	B1
<b>C</b>	A5	A4	B4	B3
<b>D</b>	A7	B6	A6	B5
<b>E</b>	GND	A8	B8	B7

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	6.5	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	6.5	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	6.5	V
V <sub>O</sub>	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-50	mA
I <sub>O</sub>	Continuous output current		±50	mA
	Continuous current through V <sub>CC</sub> or GND		±100	mA

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* table.

### 7.2 Handling Ratings

		MIN	MAX	UNIT	
T <sub>stg</sub>	Storage temperature range	-65	150	°C	
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	0	1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN54LVCH245A		SN74LVCH245A		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	Operating		2	3.6	V
		Data retention only		1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V			0.65 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V			1.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V		2	2	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V			0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V			0.7	
		V <sub>CC</sub> = 2.7 V to 3.6 V			0.8	
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	High or low state		0	V <sub>CC</sub>	V
		3-state		0	5.5	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V			-4	mA
		V <sub>CC</sub> = 2.3 V			-8	
		V <sub>CC</sub> = 2.7 V			-12	
		V <sub>CC</sub> = 3 V			-24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V			4	mA
		V <sub>CC</sub> = 2.3 V			8	
		V <sub>CC</sub> = 2.7 V		12	12	
		V <sub>CC</sub> = 3 V		24	24	
Δt/Δv	Input transition rise or fall rate		10		10	ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	125	°C

(1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, (SCBA004).

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74LVCH245A							UNIT	
	DB	DGV	DW	GQN or ZQN	NS	PW	RGY		
	20 PINS								
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	94.5	114.7	88.3	129.3	74.7	102.5	41.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	56.2	29.8	51.1	75.3	40.5	35.9	47.7	
R <sub>θJB</sub>	Junction-to-board thermal resistance	49.7	56.2	50.9	77.6	42.3	53.5	17.1	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	18.1	0.8	20.0	2.6	14.3	2.2	1.4	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	49.2	55.5	50.5	73.2	41.9	52.9	17.1	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	n/a	n/a	n/a	9.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LVCH245A			–40°C TO 85°C			–40°C TO 125°C			UNIT
			SN74LVCH245A			SN74LVCH245A			SN74LVCH245A			
			MIN	TYP	MAX	MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –100 μA	1.65 V to 3.6 V				V <sub>CC</sub> – 0.2			V <sub>CC</sub> – 0.2		V	
		2.7 V to 3.6 V	V <sub>CC</sub> – 0.2									
	I <sub>OH</sub> = –4 mA	1.65 V			1.2			1.2				
	I <sub>OH</sub> = –8 mA	2.3 V			1.7			1.7				
	I <sub>OH</sub> = –12 mA	2.7 V		2.2		2.2			2.2			
		3 V		2.4		2.4			2.4			
I <sub>OH</sub> = –24 mA	3 V		2.2		2.2			2.2				
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V					0.2			0.20	V	
		2.7 V to 3.6 V			0.2							
	I <sub>OL</sub> = 4 mA	1.65 V					0.45		0.45			
	I <sub>OL</sub> = 8 mA	2.3 V					0.7		0.7			
	I <sub>OL</sub> = 12 mA	2.7 V		0.4		0.4			0.4			
	I <sub>OL</sub> = 24 mA	3 V		0.55		0.55			0.55			
I <sub>I</sub>	Control inputs	V <sub>I</sub> = 0 to 5.5 V	3.6 V							±5	μA	
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0							±10	μA	
I <sub>I(hold)</sub>	V <sub>I</sub> = 0.58 V	1.65 V				25			25		μA	
			V <sub>I</sub> = 1.07 V				–25			–25		
	V <sub>I</sub> = 0.7 V	2.3 V				45			45			
			V <sub>I</sub> = 1.7 V				–45			–45		
	V <sub>I</sub> = 0.8 V	3 V		75		75			75			
			V <sub>I</sub> = 2 V		–75		–75			–75		
V <sub>I</sub> = 0 to 3.6 V <sup>(2)</sup>	3.6 V			±500			±500		±500			
I <sub>OZ</sub> <sup>(3)</sup>		V <sub>O</sub> = 0 V or (V <sub>CC</sub> to 5.5 V)	2.3 V to 3.6 V							±15	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	I <sub>O</sub> = 0	3.6 V			10			10		μA	
				3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>(4)</sup>			10			10		
ΔI <sub>CC</sub>		One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V			500			500		μA	
C <sub>i</sub>	Control inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		4	12		4			pF	
C <sub>io</sub>	A or B port	V <sub>O</sub> = V <sub>CC</sub> or GND	3.3 V		5.5	12		5.50			pF	

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This is the bus-hold maximum dynamic current required to switch the input from one state to another.

(3) For the total leakage current in an I/O port, please consult the I<sub>I(hold)</sub> specification for the input voltage condition 0 V < V<sub>I</sub> < V<sub>CC</sub>, and the I<sub>OZ</sub> specification for the input voltage conditions V<sub>I</sub> = 0 V or V<sub>I</sub> = V<sub>CC</sub> to 5.5 V. The bus-hold current, at input voltage greater than V<sub>CC</sub>, is negligible.

(4) This applies in the disabled state only.

**SN54LVCH245A, SN74LVCH245A**

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**7.6 Switching Characteristics, SN54LVCH245A**

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVCH245A				UNIT
			V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		
			MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	B or A	8		1	7	ns
t <sub>en</sub>	$\overline{OE}$	A or B	9.5		1	8.5	ns
t <sub>dis</sub>	$\overline{OE}$	A or B	8.5		1	7.5	ns

**7.7 Switching Characteristics, SN74LVCH245A**

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVCH245A						UNIT		
			–40°C TO 85°C								
			V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V			V <sub>CC</sub> = 3.3 V ± 0.3 V	
MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MAX	MAX		
t <sub>pd</sub>	A or B	B or A	12.7		8.3		7.3		1.5	6.3	ns
t <sub>en</sub>	$\overline{OE}$	A or B	15.3		10.5		9.5		1.5	8.5	ns
t <sub>dis</sub>	$\overline{OE}$	A or B	17		9.5		8.5		1.5	7.5	ns
t <sub>sk(o)</sub>			1		1		1		1		ns

**7.8 Switching Characteristics, SN74LVCH245A**

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN74LVCH245A								UNIT
				–40°C TO 125°C								
				V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		
MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
t <sub>pd</sub>	A or B	B or A		13.7		9.1		7.8		1.5	6.7	ns
t <sub>en</sub>	$\overline{OE}$	A or B		16.8		12		10		1.5	9.1	ns
t <sub>dis</sub>	$\overline{OE}$	A or B		18		10.5		8.7		1.5	7.8	ns
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF	5.4	7.5	1	8.5	1	8.5	1	9.5	ns
t <sub>PHL</sub>				5.4	7.5	1	8.5	1	8.5	1	9.5	
t <sub>PZH</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF	6.2	9.3	1	10.5	1	10.5	1	11.5	ns
t <sub>PZL</sub>				6.2	9.3	1	10.5	1	10.5	1	11.5	
t <sub>PHZ</sub>	$\overline{OE}$	Y	C <sub>L</sub> = 50 pF	6.7	9.2	1	10.5	1	10.5	1	11	ns
t <sub>PLZ</sub>				6.7	9.2	1	10.5	1	10.5	1	11	
t <sub>sk(o)</sub>			C <sub>L</sub> = 50 pF	1 <sup>(1)</sup>		1		1		1		ns

(1) On products compliant to MIL-PRF-38535, this parameter does not apply.

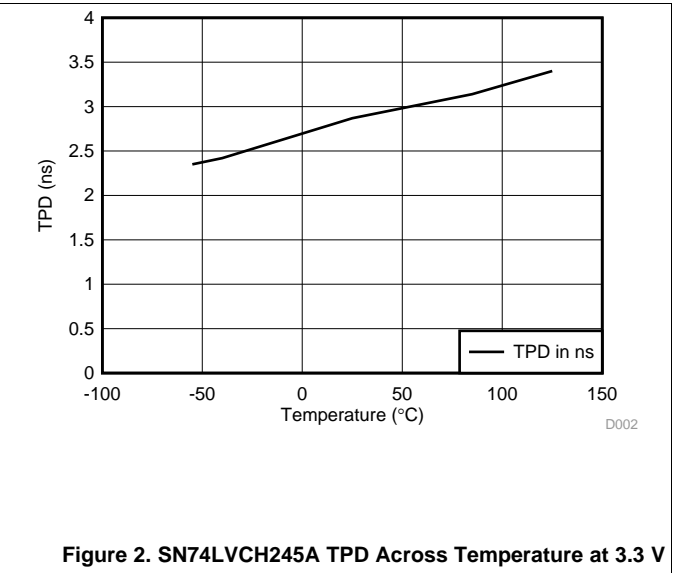
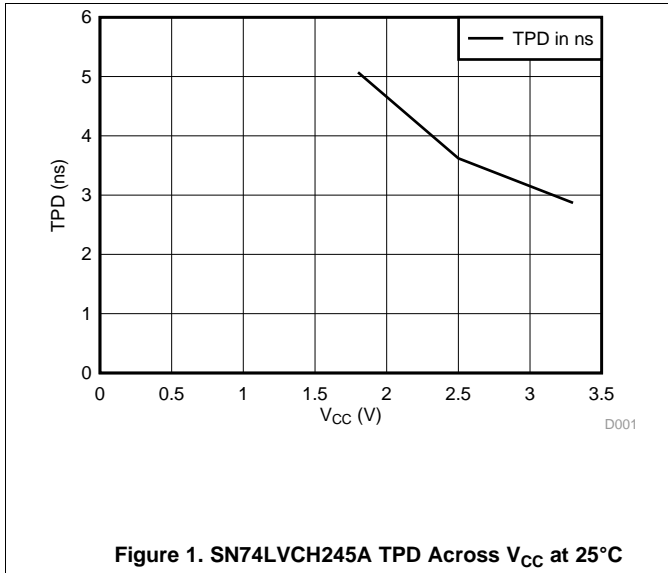
**7.9 Operating Characteristics**

 T<sub>A</sub> = 25°C

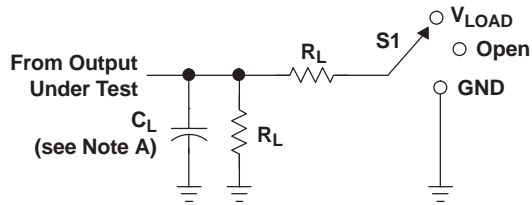
PARAMETER		TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
			TYP	TYP	TYP	
C <sub>pd</sub>	Power dissipation capacitance per transceiver	Outputs enabled	42	43	47	pF
		Outputs disabled	1	1	2	



## 7.10 Typical Characteristics

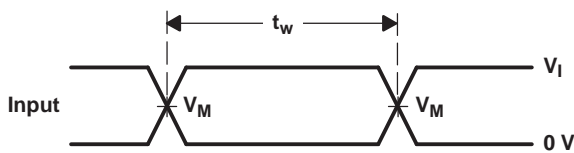
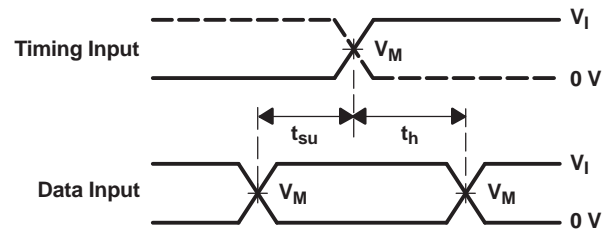
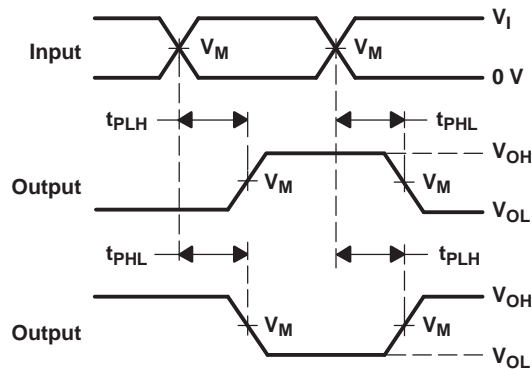
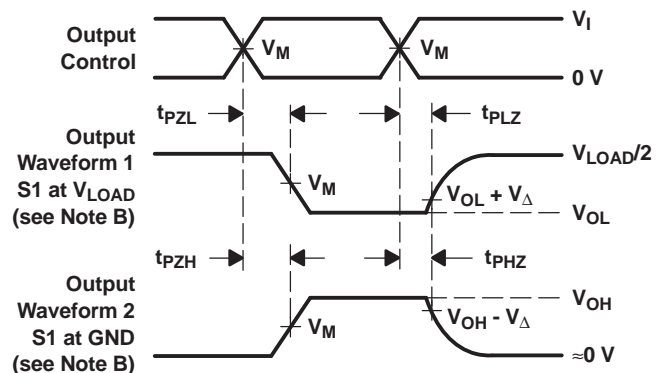


## 8 Parameter Measurement Information


**LOAD CIRCUIT**

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V


**VOLTAGE WAVEFORMS  
PULSE DURATION**

**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**

**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS**

**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING**

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - The outputs are measured one at a time with, one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**

## 9 Detailed Description

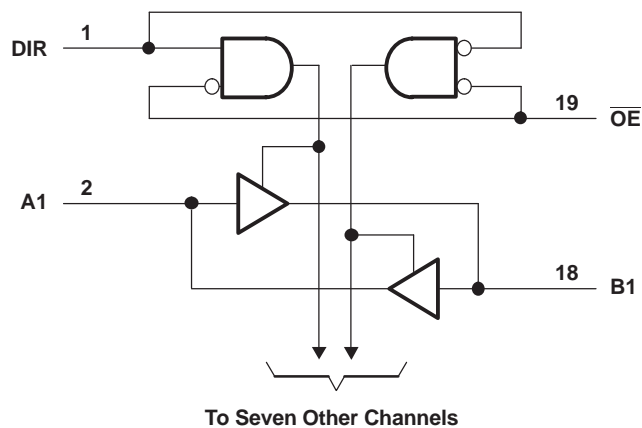
### 9.1 Overview

The SN54LVCH245A octal bus transceiver is designed for 2.7-V to 3.6-V  $V_{CC}$  operation, and the SN74LVCH245A octal bus transceiver is designed for 1.65-V to 3.6-V  $V_{CC}$  operation. Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

These devices are designed for asynchronous communication between data buses. These devices transmit data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so the buses are effectively isolated.

These devices are fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended. The bus-hold circuitry is part of the input circuit and is not disabled by  $\overline{OE}$  or DIR.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

- Wide operating voltage range from 1.65 V to 3.6 V
- Allows down voltage translation
- Inputs accept voltages to 5.5 V
- $I_{off}$  feature allows voltages on the inputs and outputs when  $V_{CC}$  is 0 V

### 9.4 Device Functional Modes

Table 2. Function Table

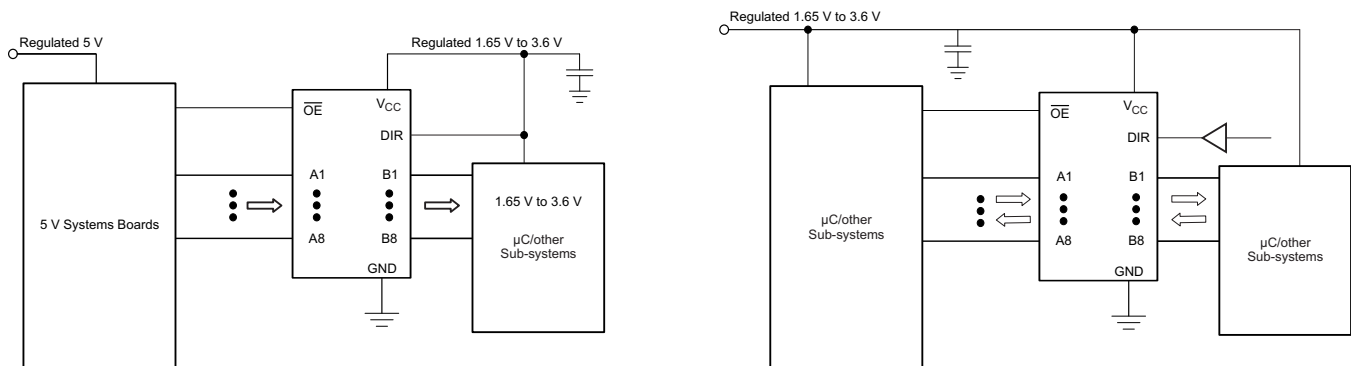
INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

## 10 Application and Implementation

### 10.1 Application Information

The SN74LVCH245A device is a high-drive CMOS device that can be used for a multitude of bus interface type applications where the data needs to be transmitted and received. It can produce 24 mA of drive current at 3.3 V. Therefore, this device is ideal for driving multiple outputs and for high-speed applications up to 100 Mhz. The inputs are 5.5-V tolerant allowing the devices to translate down to  $V_{CC}$ .

### 10.2 Typical Application



**Figure 4. Typical Application Diagram**

#### 10.2.1 Design Requirements

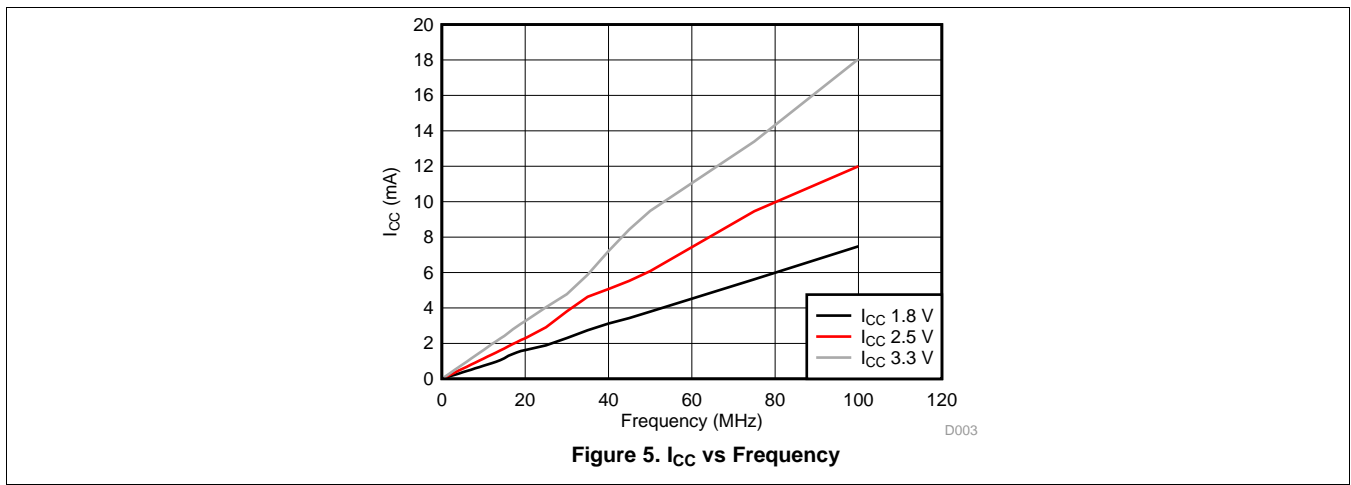
This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

#### 10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
  - Rise time and fall time specs: See  $(\Delta t/\Delta V)$  in the [Recommended Operating Conditions](#) table.
  - Specified high and low levels: See  $(V_{IH}$  and  $V_{IL})$  in the [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
2. Recommend Output Conditions
  - Load currents should not exceed 25 mA per output and 50 mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

## Typical Application (continued)

### 10.2.3 Application Curves



## 11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{f}$  is recommended; if there are multiple  $V_{CC}$  pins, then 0.01  $\mu\text{f}$  or 0.022  $\mu\text{f}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{f}$  and a 1  $\mu\text{f}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 12 Layout

### 12.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 6](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

### 12.2 Layout Example

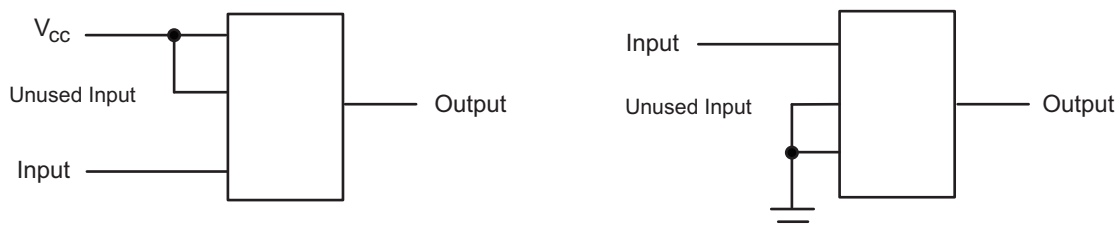


Figure 6. Layout Diagram

## 13 Device and Documentation Support

### 13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 3. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LVCH245A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SN74LVCH245A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 13.2 Trademarks

All trademarks are the property of their respective owners.

### 13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9754301Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9754301Q2A SNJ54LVCH 245AFK	<a href="#">Samples</a>
5962-9754301QRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9754301QR A SNJ54LVCH245AJ	<a href="#">Samples</a>
5962-9754301QSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9754301QS A SNJ54LVCH245AW	<a href="#">Samples</a>
5962-9754301V2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9754301V2A SNV54LVCH 245AFK	<a href="#">Samples</a>
5962-9754301VRA	ACTIVE	CDIP	J	20	20	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9754301VR A SNV54LVCH245AJ	<a href="#">Samples</a>
5962-9754301VSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9754301VS A SNV54LVCH245AW	<a href="#">Samples</a>
SN74LVCH245ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH245A	<a href="#">Samples</a>
SN74LVCH245ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH245A	<a href="#">Samples</a>
SN74LVCH245ADGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH245A	<a href="#">Samples</a>
SN74LVCH245ADGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH245A	<a href="#">Samples</a>
SN74LVCH245ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH245A	<a href="#">Samples</a>
SN74LVCH245ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH245A	<a href="#">Samples</a>
SN74LVCH245ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH245A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVCH245ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVCH245A	<a href="#">Samples</a>
SN74LVCH245APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH245A	<a href="#">Samples</a>
SN74LVCH245APWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH245A	<a href="#">Samples</a>
SN74LVCH245APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-40 to 85	LCH245A	<a href="#">Samples</a>
SN74LVCH245APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH245A	<a href="#">Samples</a>
SN74LVCH245APWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH245A	<a href="#">Samples</a>
SN74LVCH245APWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH245A	<a href="#">Samples</a>
SN74LVCH245APWTG4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCH245A	<a href="#">Samples</a>
SN74LVCH245ARGYR	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LCH245A	<a href="#">Samples</a>
SN74LVCH245ARGYRG4	ACTIVE	VQFN	RGY	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LCH245A	<a href="#">Samples</a>
SN74LVCH245AZQNR	ACTIVE	BGA MICROSTAR JUNIOR	ZQN	20	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	LCH245A	<a href="#">Samples</a>
SN74LVCH245AZXYR	ACTIVE	BGA MICROSTAR JUNIOR	ZXY	20	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	KH245A	<a href="#">Samples</a>
SNJ54LVCH245AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9754301Q2A SNJ54LVCH 245AFK	<a href="#">Samples</a>
SNJ54LVCH245AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9754301QR A SNJ54LVCH245AJ	<a href="#">Samples</a>
SNJ54LVCH245AW	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9754301QS A SNJ54LVCH245AW	<a href="#">Samples</a>



(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LVCH245A, SN54LVCH245A-SP, SN74LVCH245A :**

● Catalog: [SN74LVCH245A](#), [SN54LVCH245A](#)

● Military: [SN54LVCH245A](#)

- Space: [SN54LVCH245A-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCH245ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74LVCH245ADGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVCH245ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74LVCH245ANSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74LVCH245APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVCH245APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVCH245APWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVCH245APWT	TSSOP	PW	20	250	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74LVCH245ARGYR	VQFN	RGY	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1
SN74LVCH245AZQNR	BGA MICROSTAR JUNIOR	ZQN	20	1000	330.0	12.4	3.3	4.3	1.6	8.0	12.0	Q1
SN74LVCH245AZXYR	BGA MICROSTAR JUNIOR	ZXY	20	2500	330.0	12.4	2.8	3.3	1.0	4.0	12.0	Q2

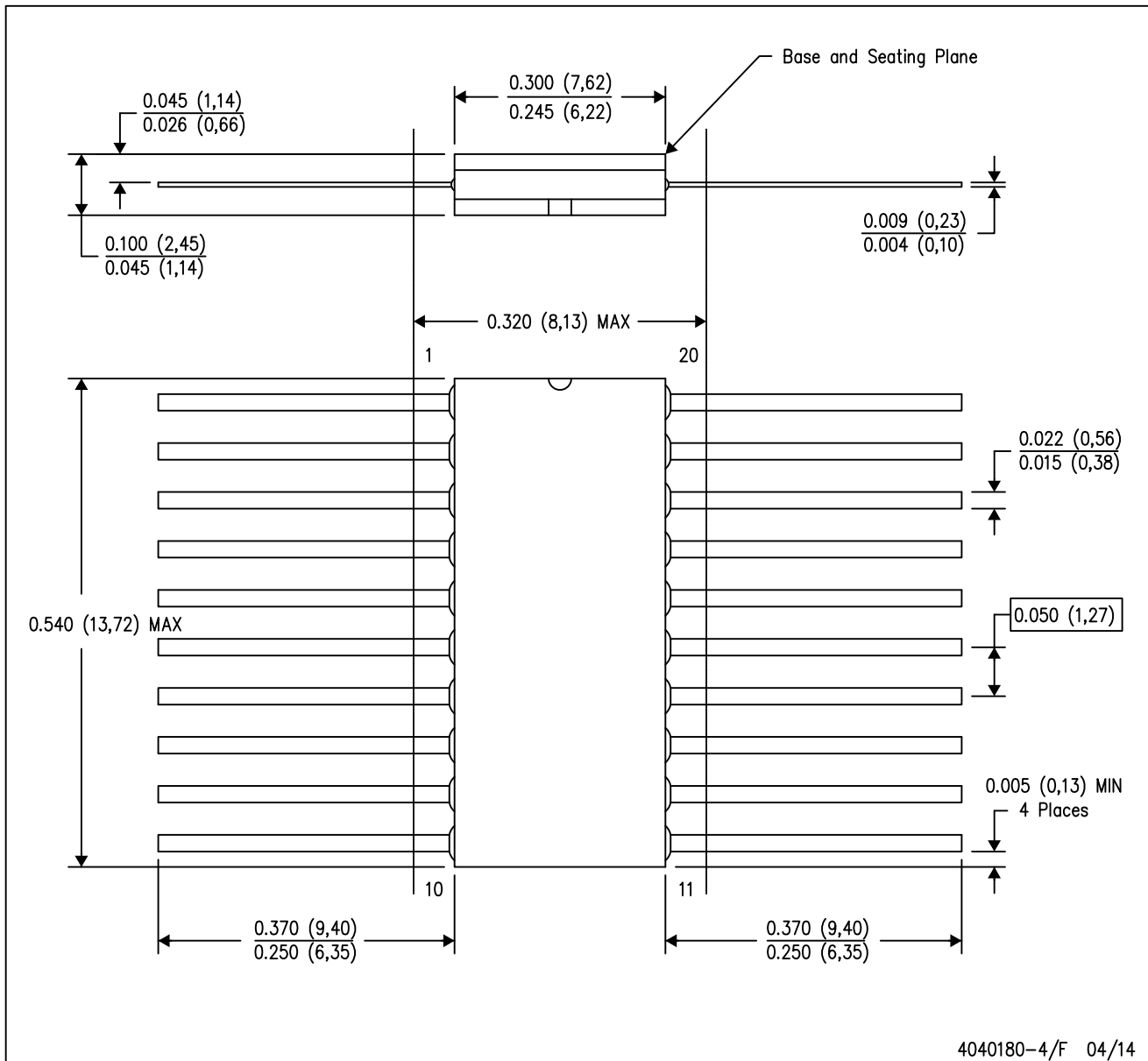
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCH245ADBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74LVCH245ADGVR	TVSOP	DGV	20	2000	367.0	367.0	35.0
SN74LVCH245ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74LVCH245ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74LVCH245APWR	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74LVCH245APWR	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74LVCH245APWRG4	TSSOP	PW	20	2000	367.0	367.0	38.0
SN74LVCH245APWT	TSSOP	PW	20	250	367.0	367.0	38.0
SN74LVCH245ARGYR	VQFN	RGY	20	3000	367.0	367.0	35.0
SN74LVCH245AZQNR	BGA MICROSTAR JUNIOR	ZQN	20	1000	336.6	336.6	28.6
SN74LVCH245AZXYR	BGA MICROSTAR JUNIOR	ZXY	20	2500	336.6	336.6	28.6

W (R-GDFP-F20)

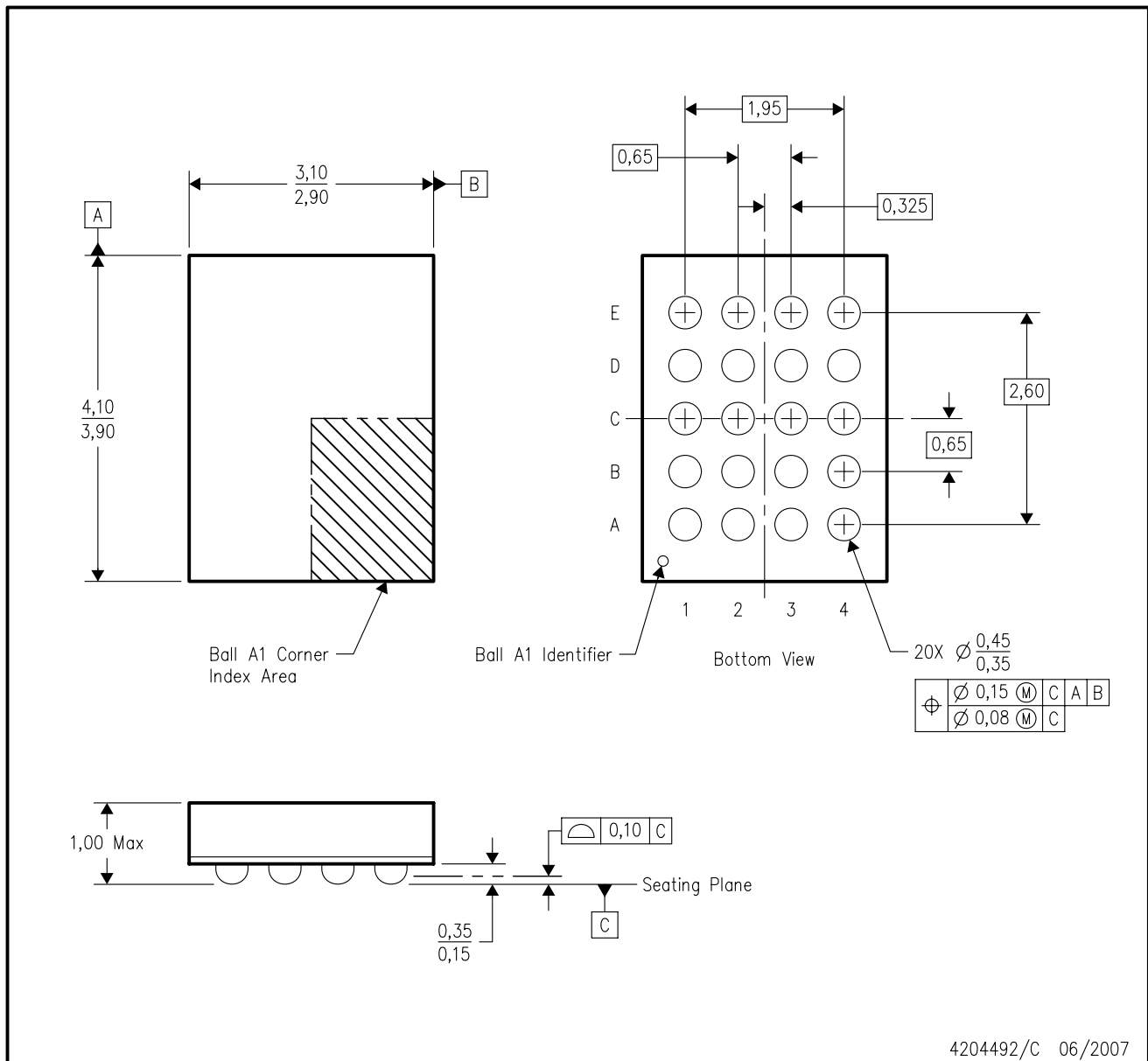
CERAMIC DUAL FLATPACK



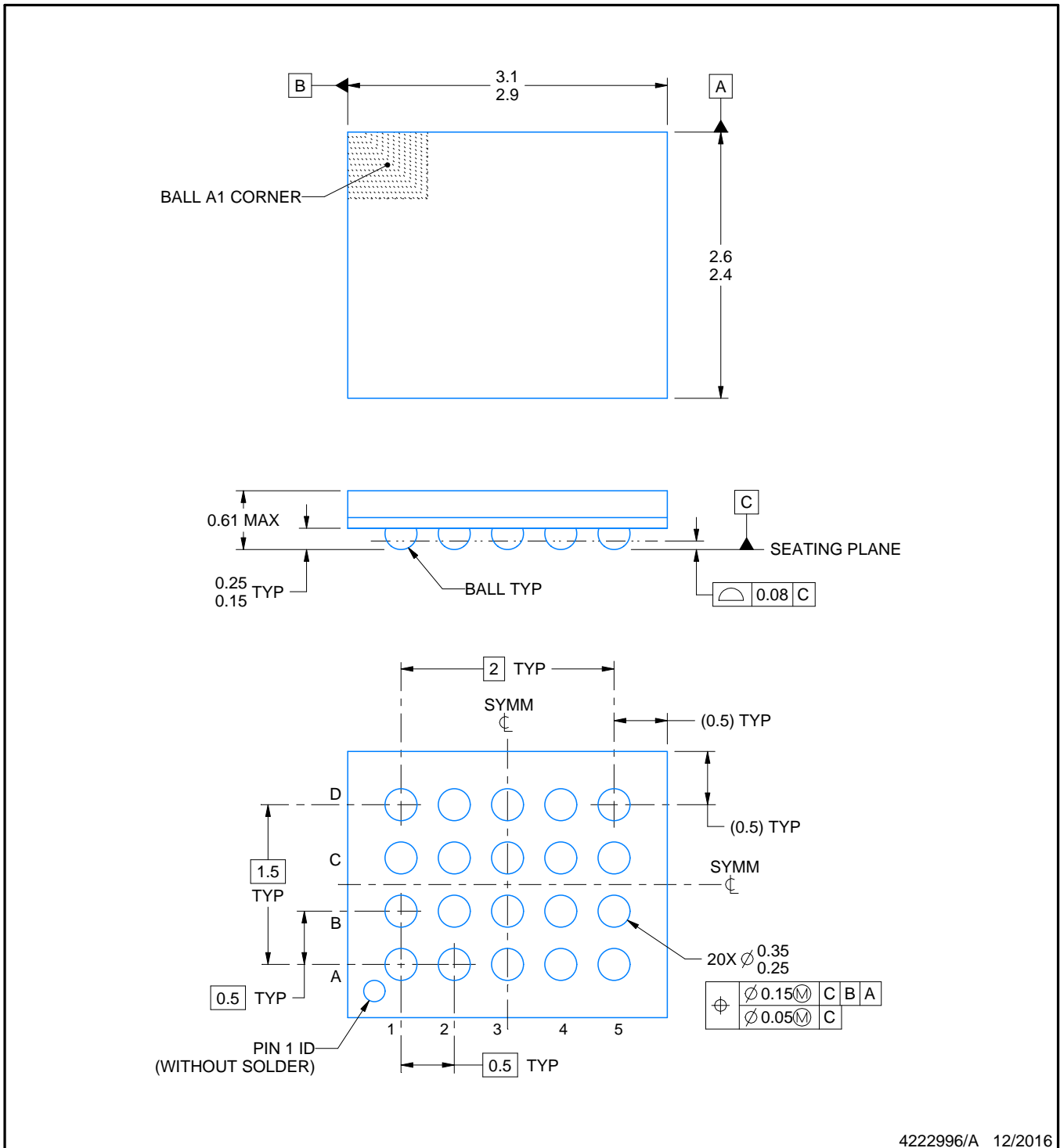
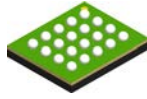
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

ZQN (R-PBGA-N20)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-285 variation BC-2.
  - D. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead (SnPb).



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NOTES:

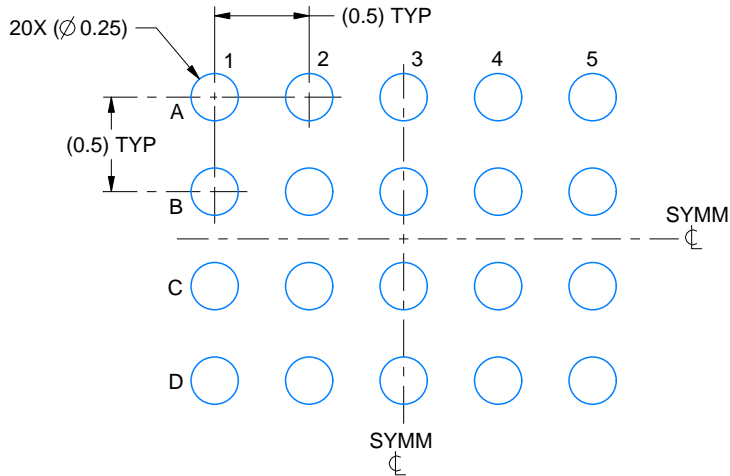
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

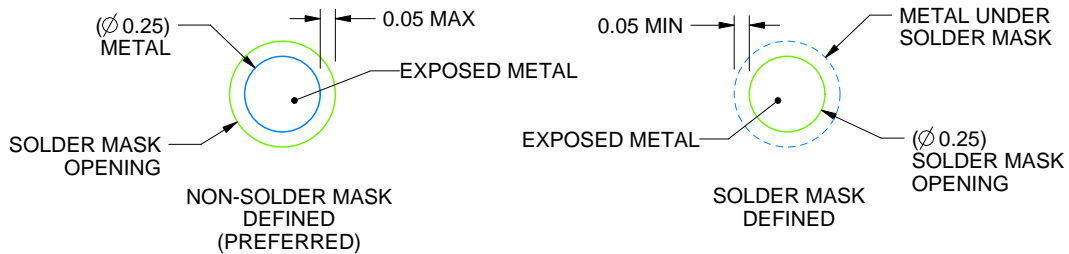
ZXY0020A

VFBGA - 0.61 mm max height

PLASTIC BALL GRID ARRAY



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:25X



SOLDER MASK DETAILS  
NOT TO SCALE

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NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 ([www.ti.com/lit/spraa99](http://www.ti.com/lit/spraa99)).

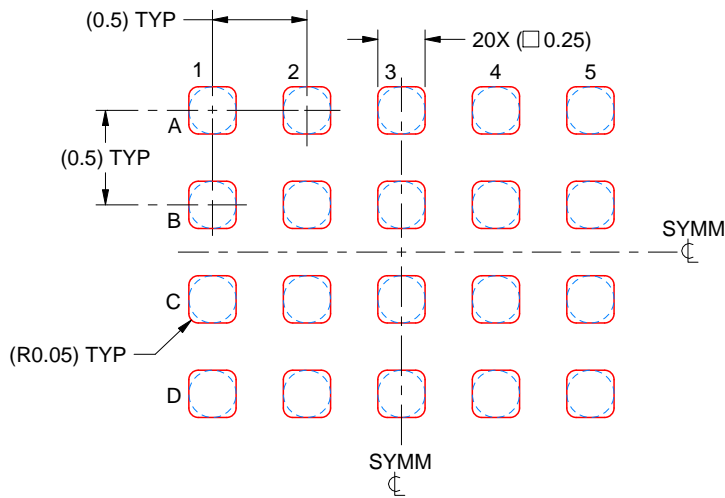


# EXAMPLE STENCIL DESIGN

ZXY0020A

VFBGA - 0.61 mm max height

PLASTIC BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE: 25X

4222996/A 12/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)




4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  -  Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - G. Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N20)

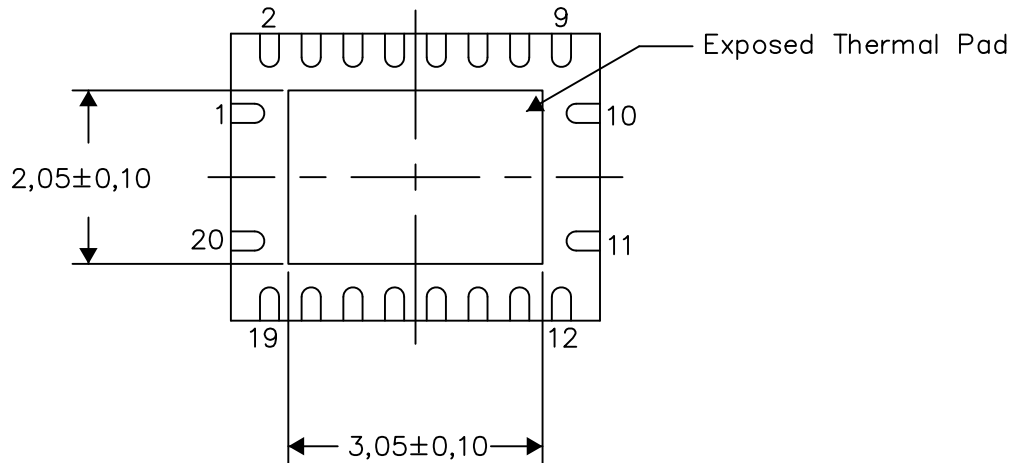
PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-4/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194





PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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