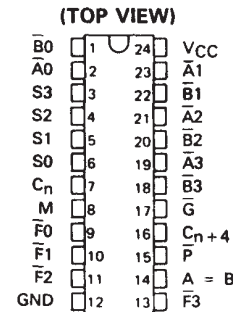


SN54LS181, SN54S181 SN74LS181, SN74S181 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

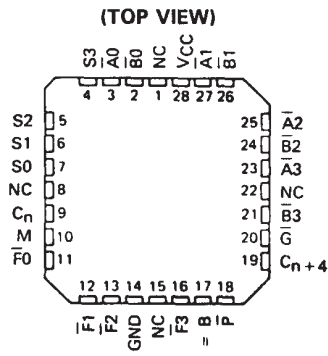
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- Full Look-Ahead for High-Speed Operations on Long Words
- Input Clamping Diodes Minimize Transmission-Line Effects
- Darlington Outputs Reduce Turn-Off Time
- Arithmetic Operating Modes:
 - Addition
 - Subtraction
 - Shift Operand A One Position
 - Magnitude Comparison
 - Plus Twelve Other Arithmetic Operations
- Logic Function Modes:
 - Exclusive-OR
 - Comparator
 - AND, NAND, OR, NOR
 - Plus Ten Other Logic Operations

SN54LS181, SN54S181 . . . J OR W PACKAGE
SN74LS181, SN74S181 . . . DW OR N PACKAGE



SN54LS181, SN54S181 . . . FK PACKAGE



NC - No internal connection

TYPICAL ADDITION TIMES

| NUMBER OF BITS | ADDITION TIMES | | PACKAGE COUNT | | CARRY METHOD BETWEEN ALUs |
|----------------|------------------------|-----------------------|-------------------------|-----------------------------|---------------------------|
| | USING 'LS181 AND 'S182 | USING 'S181 AND 'S182 | ARITHMETIC/ LOGIC UNITS | LOOK-AHEAD CARRY GENERATORS | |
| 1 to 4 | 24 ns | 11 ns | 1 | | NONE |
| 5 to 8 | 40 ns | 18 ns | 2 | | RIPPLE |
| 9 to 16 | 44 ns | 19 ns | 3 or 4 | 1 | FULL LOOK-AHEAD |
| 17 to 64 | 68 ns | 28 ns | 5 to 16 | 2 to 5 | FULL LOOK-AHEAD |

description

The 'LS181 and 'S181 are arithmetic logic units (ALU)/function generators that have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the SN54S182 or SN74S182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown above illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading 'S182 circuits with these ALUs to provide multi-level full carry look-ahead is illustrated under typical applications data for the 'S182.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output ($C_n + 4$) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



**SN54LS181, SN54S181
SN74LS181, SN74S181
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS**

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description (continued)

The 'LS181 and 'S181 will accommodate active-high data if the pin designations are interpreted as follows:

| PIN NUMBER | 2 | 1 | 23 | 22 | 21 | 20 | 19 | 18 | 9 | 10 | 11 | 13 | 7 | 16 | 15 | 17 |
|----------------------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-------------|-----------------|-----------|-----------|
| Active-low data (Table 1) | \bar{A}_0 | \bar{B}_0 | \bar{A}_1 | \bar{B}_1 | \bar{A}_2 | \bar{B}_2 | \bar{A}_3 | \bar{B}_3 | \bar{F}_0 | \bar{F}_1 | \bar{F}_2 | \bar{F}_3 | C_n | C_{n+4} | \bar{P} | \bar{G} |
| Active-high data (Table 2) | A ₀ | B ₀ | A ₁ | B ₁ | A ₂ | B ₂ | A ₃ | B ₃ | F ₀ | F ₁ | F ₂ | F ₃ | \bar{C}_n | \bar{C}_{n+4} | X | Y |

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is $A-B-1$, which requires an end-around or forced carry to provide $A-B$.

The 'LS181 or 'S181 can also be utilized as a comparator. The $A = B$ output is internally decoded from the function outputs (F_0, F_1, F_2, F_3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality ($A=B$). The ALU must be in the subtract mode with $C_n = H$ when performing this comparison. The $A = B$ output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU must be placed in the subtract mode by placing the function select inputs S_3, S_2, S_1, S_0 at L, H, H, L, respectively.

| INPUT C_n | OUTPUT C_{n+4} | ACTIVE-LOW DATA (FIGURE 1) | ACTIVE-HIGH DATA (FIGURE 2) |
|-------------|------------------|-------------------------------|--------------------------------|
| H | H | $A > B$ | $A < B$ |
| H | L | $A < B$ | $A > B$ |
| L | H | $A > B$ | $A < B$ |
| L | L | $A < B$ | $A > B$ |

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S_0, S_1, S_2, S_3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

Series 54, 54LS, and 54S devices are characterized for operation over the full military temperature range of -55°C to 125°C ; Series 74LS and 74S devices are characterized for operation from 0°C to 70°C .

signal designations

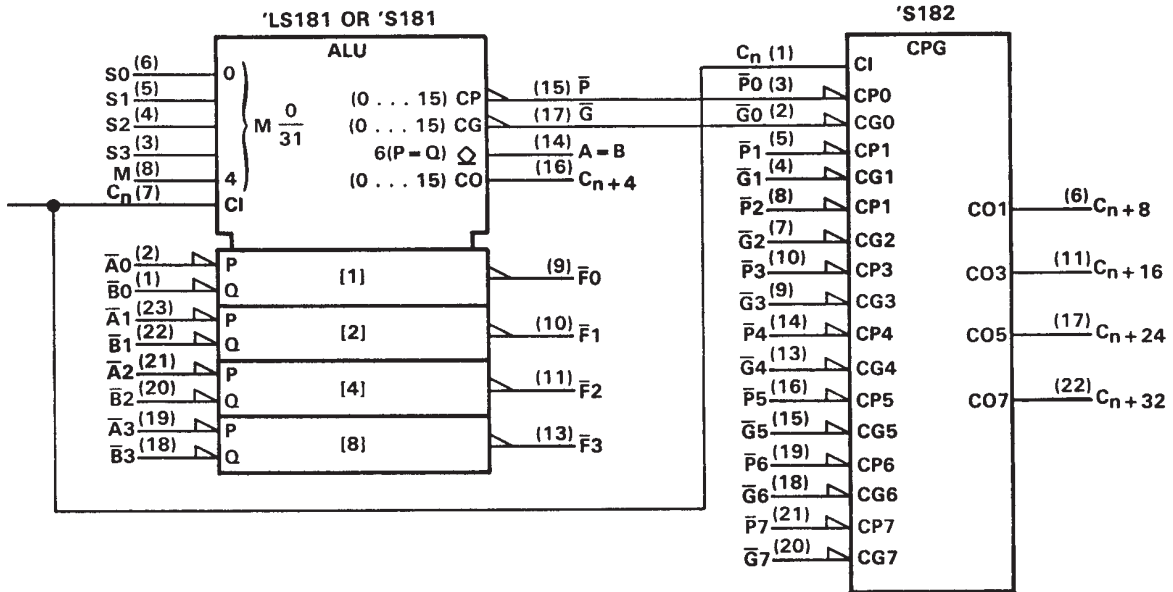
In both Figures 1 and 2, the polarity indicators (∇) indicate that the associated input or output is active-low with respect to the function shown inside the symbol, and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data, and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations have been changed in Figure 2 to accommodate the logic functions and arithmetic operations for the active-high data given in Table 2. The 'LS181 and 'S181, together with the 'S182, can be used with the signal designation of either Figure 1 or Figure 2.



SN54LS181, SN54S181
SN74LS181, SN74S181
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logic symbols† and signal designations (active-low data)



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for dual-in-line and "small outline" packages.

FIGURE 1 (USE WITH TABLE 1)

TABLE 1

| SELECTION | | | | ACTIVE-LOW DATA | | |
|-----------|----|----|----|-----------------------------|-----------------------------------|--|
| | | | | M = H LOGIC FUNCTIONS | M = L; ARITHMETIC OPERATIONS | |
| S3 | S2 | S1 | S0 | | Cn = L (no carry) | Cn = H (with carry) |
| L | L | L | L | $F = \overline{A}$ | F = A MINUS 1 | F = A |
| L | L | L | H | $F = \overline{AB}$ | F = AB MINUS 1 | F = AB |
| L | L | H | L | $F = \overline{A + B}$ | F = \overline{AB} MINUS 1 | F = \overline{AB} |
| L | L | H | H | F = 1 | F = MINUS 1 (2's COMP) | F = ZERO |
| L | H | L | L | $F = \overline{A + B}$ | F = A PLUS (A + \overline{B}) | F = A PLUS (A + \overline{B}) PLUS 1 |
| L | H | L | H | $F = \overline{B}$ | F = AB PLUS (A + \overline{B}) | F = AB PLUS (A + \overline{B}) PLUS 1 |
| L | H | H | L | $F = A \oplus B$ | F = A MINUS B MINUS 1 | F = A MINUS B |
| L | H | H | H | $F = A + \overline{B}$ | $F = A + \overline{B}$ | F = (A + \overline{B}) PLUS 1 |
| H | L | L | L | $F = \overline{AB}$ | F = A PLUS (A + B) | F = A PLUS (A + B) PLUS 1 |
| H | L | L | H | $F = A \oplus B$ | F = A PLUS B | F = A PLUS B PLUS 1 |
| H | L | H | L | F = B | F = \overline{AB} PLUS (A + B) | F = \overline{AB} PLUS (A + B) PLUS 1 |
| H | L | H | H | F = A + B | F = (A + B) | F = (A + B) PLUS 1 |
| H | H | L | L | F = 0 | F = A PLUS A ‡ | F = A PLUS A PLUS 1 |
| H | H | L | H | $F = \overline{AB}$ | F = AB PLUS A | F = AB PLUS A PLUS 1 |
| H | H | H | L | F = AB | F = \overline{AB} PLUS A | F = \overline{AB} PLUS A PLUS 1 |
| H | H | H | H | F = A | F = A | F = A PLUS 1 |

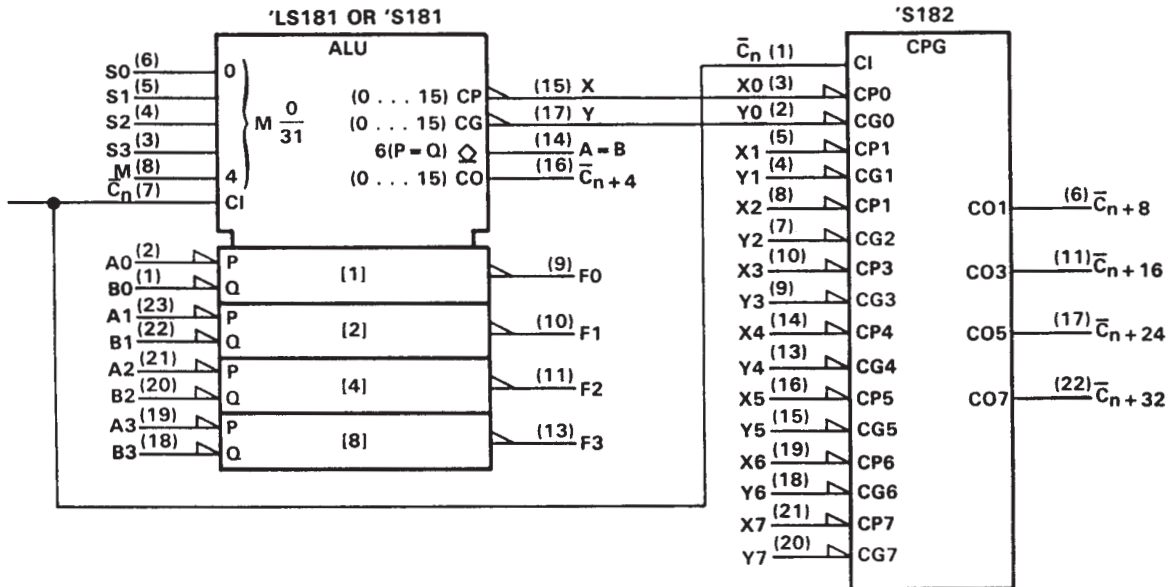
‡Each bit is shifted to the next more significant position.



SN54LS181, SN54S181
 SN74LS181, SN74S181
 ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

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logic symbols† and signal designations (active-high data)



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for dual-in-line and "small outline" packages.

FIGURE 2 (USE WITH TABLE 2)

TABLE 2

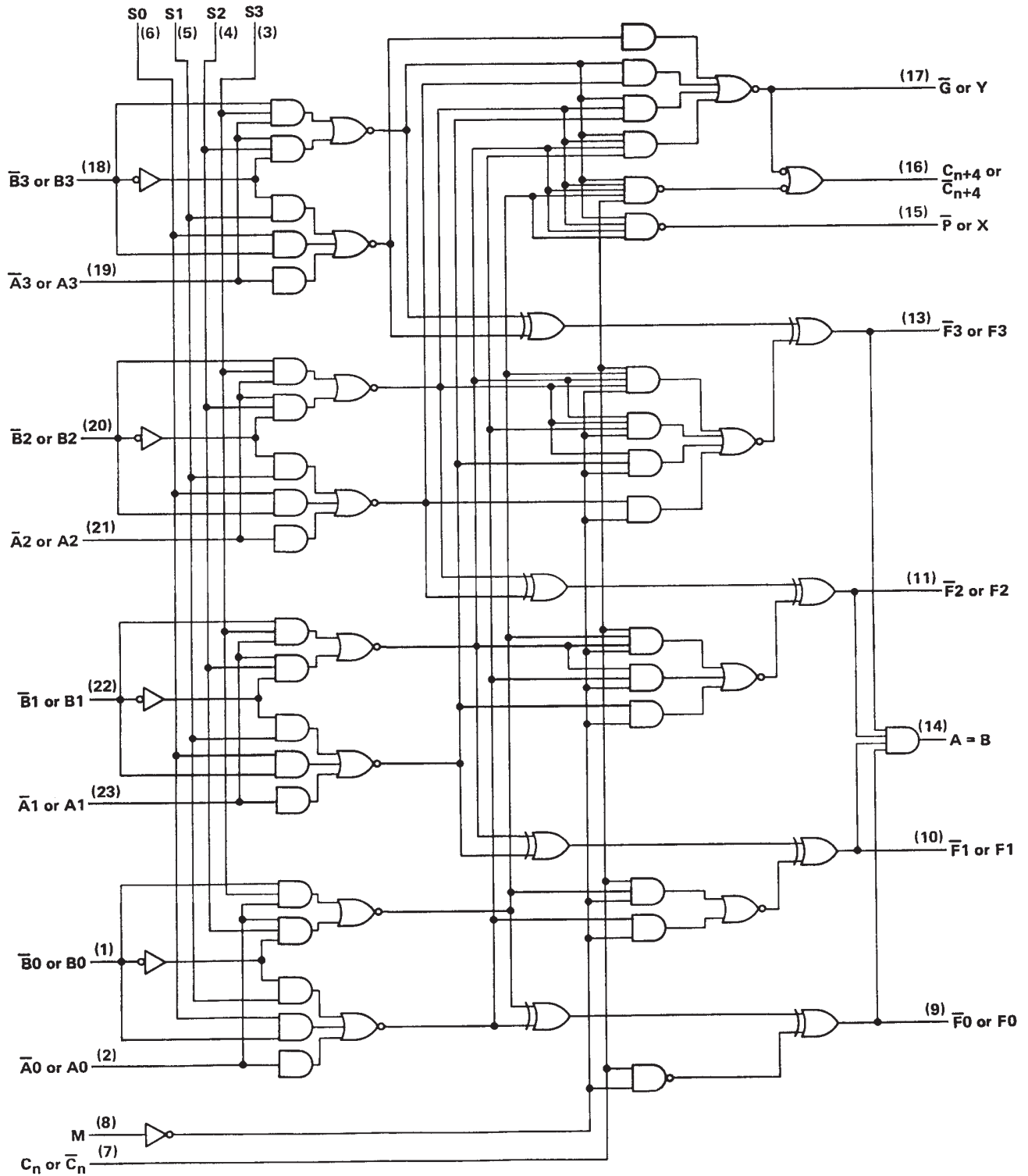
| SELECTION | | | | ACTIVE-HIGH DATA | | |
|-----------|----|----|----|-----------------------------|--|--|
| | | | | M = H LOGIC FUNCTIONS | M = L; ARITHMETIC OPERATIONS | |
| S3 | S2 | S1 | S0 | | $\bar{C}_n = H$ (no carry) | $\bar{C}_n = L$ (with carry) |
| L | L | L | L | $F = \bar{A}$ | $F = A$ | $F = A \text{ PLUS } 1$ |
| L | L | L | H | $F = \bar{A} + B$ | $F = A + B$ | $F = (A + B) \text{ PLUS } 1$ |
| L | L | H | L | $F = \bar{A}B$ | $F = A + \bar{B}$ | $F = (A + \bar{B}) \text{ PLUS } 1$ |
| L | L | H | H | $F = 0$ | $F = \text{MINUS } 1 \text{ (2's COMPL)}$ | $F = \text{ZERO}$ |
| L | H | L | L | $F = \bar{A}B$ | $F = A \text{ PLUS } \bar{A}\bar{B}$ | $F = A \text{ PLUS } \bar{A}\bar{B} \text{ PLUS } 1$ |
| L | H | L | H | $F = \bar{B}$ | $F = (A + B) \text{ PLUS } \bar{A}\bar{B}$ | $F = (A + B) \text{ PLUS } \bar{A}\bar{B} \text{ PLUS } 1$ |
| L | H | H | L | $F = A \oplus B$ | $F = A \text{ MINUS } B \text{ MINUS } 1$ | $F = A \text{ MINUS } B$ |
| L | H | H | H | $F = \bar{A}\bar{B}$ | $F = \bar{A}\bar{B} \text{ MINUS } 1$ | $F = \bar{A}\bar{B}$ |
| H | L | L | L | $F = \bar{A} + B$ | $F = A \text{ PLUS } AB$ | $F = A \text{ PLUS } AB \text{ PLUS } 1$ |
| H | L | L | H | $F = A \oplus B$ | $F = A \text{ PLUS } B$ | $F = A \text{ PLUS } B \text{ PLUS } 1$ |
| H | L | H | L | $F = B$ | $F = (A + \bar{B}) \text{ PLUS } AB$ | $F = (A + \bar{B}) \text{ PLUS } AB \text{ PLUS } 1$ |
| H | L | H | H | $F = AB$ | $F = AB \text{ MINUS } 1$ | $F = AB$ |
| H | H | L | L | $F = 1$ | $F = A \text{ PLUS } A^\dagger$ | $F = A \text{ PLUS } A \text{ PLUS } 1$ |
| H | H | L | H | $F = A + \bar{B}$ | $F = (A + B) \text{ PLUS } A$ | $F = (A + B) \text{ PLUS } A \text{ PLUS } 1$ |
| H | H | H | L | $F = A + B$ | $F = (A + \bar{B}) \text{ PLUS } A$ | $F = (A + \bar{B}) \text{ PLUS } A \text{ PLUS } 1$ |
| H | H | H | H | $F = A$ | $F = A \text{ MINUS } 1$ | $F = A$ |

† Each bit is shifted to the next more significant position.

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 SN74LS181, SN74S181
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logic diagram (positive logic)



Pin numbers shown are for DW, J, N, and W packages.

**SN54LS181, SN54S181
SN74LS181, SN74S181
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absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)

| | |
|---|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage | 5.5 V |
| Interemitter voltage (see Note 2) | 5.5 V |
| Operating free-air temperature range: SN54LS181 | -55°C to 125°C |
| SN74LS181 | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each \bar{A} input in conjunction with inputs S2 or S3, and to each \bar{B} input in conjunction with inputs S0 or S3.

recommended operating conditions

| | SN54LS181 | | | SN74LS181 | | | UNIT |
|--|-----------|-----|------|-----------|-----|------|---------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, V_{CC} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, I_{OH} (All outputs except A = B) | | | -400 | | | -400 | μ A |
| Low-level output current, I_{OL} | | | 4 | | | 8 | mA |
| Operating free-air temperature, T_A | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | SN54LS181 | | | SN74LS181 | | | UNIT |
|-----------|---|---|----------------------------------|------|------|-----------|------|---------|---------|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V_{IH} | High-level input voltage | | 2 | | | 2 | | | V |
| V_{IL} | Low-level input voltage | | | | 0.7 | | | 0.8 | V |
| V_{IK} | Input clamp voltage | $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$ | | | -1.5 | | | -1.5 | V |
| V_{OH} | High-level output voltage, any output except A = B | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$ | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| I_{OH} | High-level output current, A = B output only | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{OH} = 5.5 \text{ V}$ | | 100 | | | 100 | | μ A |
| V_{OL} | Low-level output voltage | All outputs $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$ | $I_{OL} = 4 \text{ mA}$ | | 0.25 | 0.4 | 0.25 | 0.4 | V |
| | | | $I_{OL} = 8 \text{ mA}$ | | | | 0.35 | 0.5 | |
| | | | $I_{OL} = 16 \text{ mA}$ | | 0.47 | 0.7 | 0.47 | 0.7 | |
| | | | $I_{OL} = 8 \text{ mA}$ | | 0.35 | 0.6 | 0.35 | 0.5 | |
| I_I | Input current at max. input voltage | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$ | Mode input | | 0.1 | | 0.1 | mA | |
| | | | Any \bar{A} or \bar{B} input | | 0.3 | | 0.3 | | |
| | | | Any S input | | 0.4 | | 0.4 | | |
| | | | Carry input | | 0.5 | | 0.5 | | |
| I_{IH} | High-level input current | $V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$ | Mode input | | 20 | | 20 | μ A | |
| | | | Any \bar{A} or \bar{B} input | | 60 | | 60 | | |
| | | | Any S input | | 80 | | 80 | | |
| | | | Carry input | | 100 | | 100 | | |
| I_{IL} | Low-level input current | $V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$ | Mode input | | -0.4 | | -0.4 | mA | |
| | | | Any \bar{A} or \bar{B} input | | -1.2 | | -1.2 | | |
| | | | Any S input | | -1.6 | | -1.6 | | |
| | | | Carry input | | -2 | | -2 | | |
| I_{OS} | Short-circuit output current, any output except A = B § | $V_{CC} = \text{MAX}$ | -6 | -40 | -5 | -42 | mA | | |
| I_{CC} | Supply current | $V_{CC} = \text{MAX},$ See Note 3 | Condition A | | 20 | 32 | 20 | 34 | mA |
| | | | Condition B | | 21 | 35 | 21 | 37 | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 3: With outputs open, I_{CC} is measured for the following conditions:

- A. S0 through S3, M, and \bar{A} inputs are at 4.5 V, all other inputs are grounded.
- B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.



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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, ($C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$, see note 4)

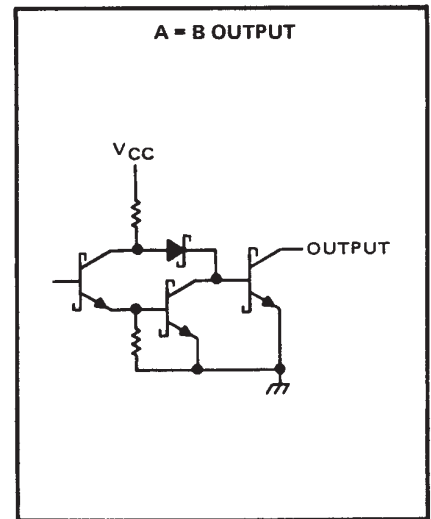
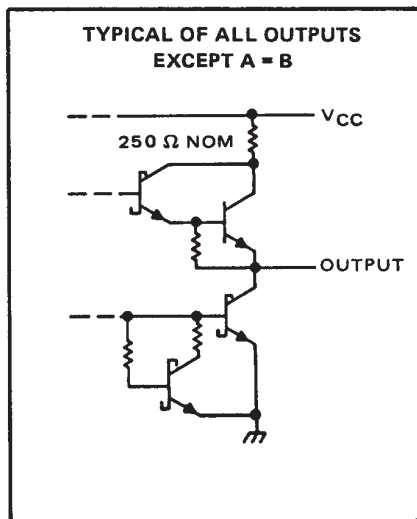
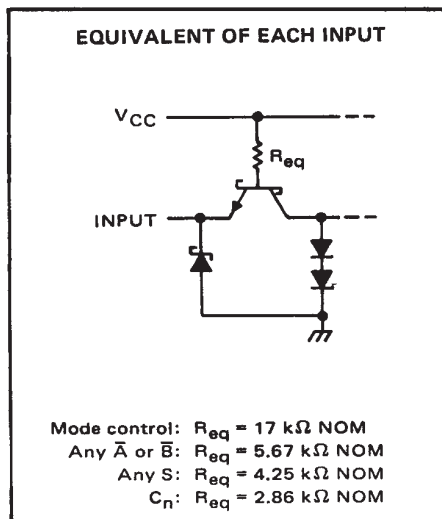
| PARAMETER† | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------|----------------------------|------------------|--|-----|-----|-----|------|
| t _{PLH} | C _n | C _{n+4} | | 18 | 27 | | ns |
| t _{PHL} | | | | 13 | 20 | | |
| t _{PLH} | Any \bar{A} or \bar{B} | C _{n+4} | M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V (SUM mode) | 25 | 38 | | ns |
| t _{PHL} | | | | 25 | 38 | | |
| t _{PLH} | Any \bar{A} or \bar{B} | C _{n+4} | M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V (DIFF mode) | 27 | 41 | | ns |
| t _{PHL} | | | | 27 | 41 | | |
| t _{PLH} | C _n | Any \bar{F} | M = 0 V (SUM or DIFF mode) | 17 | 26 | | ns |
| t _{PHL} | | | | 13 | 20 | | |
| t _{PLH} | Any \bar{A} or \bar{B} | \bar{G} | M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V (SUM mode) | 19 | 29 | | ns |
| t _{PHL} | | | | 15 | 23 | | |
| t _{PLH} | Any \bar{A} or \bar{B} | \bar{G} | M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode) | 21 | 32 | | ns |
| t _{PHL} | | | | 21 | 32 | | |
| t _{PLH} | Any \bar{A} or \bar{B} | \bar{P} | M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V, (SUM mode) | 20 | 30 | | ns |
| t _{PHL} | | | | 20 | 30 | | |
| t _{PLH} | Any \bar{A} or \bar{B} | \bar{P} | M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode) | 20 | 30 | | ns |
| t _{PHL} | | | | 22 | 33 | | |
| t _{PLH} | \bar{A}_i or \bar{B}_i | \bar{F}_i | M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V (SUM mode) | 21 | 32 | | ns |
| t _{PHL} | | | | 13 | 20 | | |
| t _{PLH} | \bar{A}_i or \bar{B}_i | \bar{F}_i | M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode) | 21 | 32 | | ns |
| t _{PHL} | | | | 21 | 32 | | |
| t _{PLH} | \bar{A}_i or \bar{B}_i | \bar{F}_i | M = 4.5 V (logic mode) | 22 | 33 | | ns |
| t _{PHL} | | | | 26 | 38 | | |
| t _{PLH} | Any \bar{A} or \bar{B} | A = B | M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode) | 33 | 50 | | ns |
| t _{PHL} | | | | 41 | 62 | | |

†t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 4: Load circuits and voltage waveforms are shown in Section 1. Refer to Parameter Measurement Information page for test conditions.

schematics of inputs and outputs



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

| | |
|--|----------------|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage | 5.5 V |
| Interemitter voltage (see Note 2) | 5.5 V |
| Operating free-air temperature: SN54S181 | -55°C to 125°C |
| SN74S181 | 0°C to 70°C |
| Storage temperature range | -65°C to 150°C |

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each \bar{A} input in conjunction with inputs S2 or S3, and to each \bar{B} input in conjunction with inputs S0 or S3.

recommended operating conditions

| | SN54S181 | | | SN74S181 | | | UNIT |
|--|----------|-----|-----|----------|-----|------|------|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, V_{CC} | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, I_{OH} (All outputs except A = B) | | | -1 | | | -1 | mA |
| Low-level output current, I_{OL} | | | 20 | | | 20 | mA |
| Operating free-air temperature, T_A | -55 | | 125 | 0 | | 70 | °C |

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | SN54S181 | | | SN74S181 | | | UNIT |
|--|---|--|--|---------|----------|---------|------|------|
| | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| V_{IH} High-level input voltage | | 2 | | | 2 | | | V |
| V_{IL} Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| V_{IK} Input clamp voltage | $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$ | | | -1.2 | | | -1.2 | V |
| V_{OH} High-level output voltage, any output except A = B | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -1 \text{ mA}$ | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| I_{OH} High-level output current, A = B output only | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, V_{OH} = 5.5 \text{ V}$ | | | 250 | | | 250 | µA |
| V_{OL} Low-level output voltage | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 20 \text{ mA}$ | | | 0.5 | | | 0.5 | V |
| I_I Input current at maximum input voltage | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$ | | | 1 | | | 1 | mA |
| I_{IH} High-level input current | Mode input | | | 50 | | | 50 | µA |
| | Any \bar{A} or \bar{B} input | $V_{CC} = \text{MAX}, V_I = 2.5 \text{ V}$ | | 150 | | | 150 | |
| | Any S input | | | 200 | | | 200 | |
| | Carry input | | | 250 | | | 250 | |
| I_{IL} Low-level input current | Mode input | | $V_{CC} = \text{MAX}, V_I = 0.5 \text{ V}$ | | -2 | | | -2 |
| | Any \bar{A} or \bar{B} input | | | -6 | | | -6 | |
| | Any S input | | | -8 | | | -8 | |
| | Carry input | | | -10 | | | -10 | |
| I_{OS} Short-circuit output current, any output except A = B § | $V_{CC} = \text{MAX}$ | | | -40 | | -100 | | mA |
| I_{CC} Supply current | $V_{CC} = \text{MAX}, T_A = 125^\circ\text{C},$ See Note 3 | W package only | | 195 | | | | mA |
| | $V_{CC} = \text{MAX},$ See Note 3 | All packages | | 120 220 | | 120 220 | | |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured for the following conditions (the typical and maximum values apply to both):

A. S0 through S3, M, and \bar{A} inputs are at 4.5 V, all other inputs are grounded, and all outputs are open.

B. S0 through S3 and M are at 4.5 V, all other inputs grounded, and all outputs are open.



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switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ ($C_L = 15\text{ pF}$, $R_L = 280\ \Omega$, see note 4)

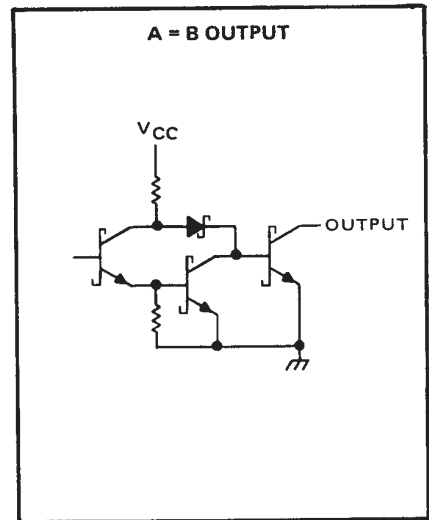
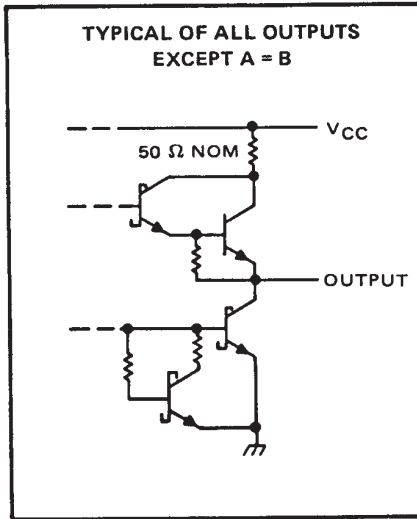
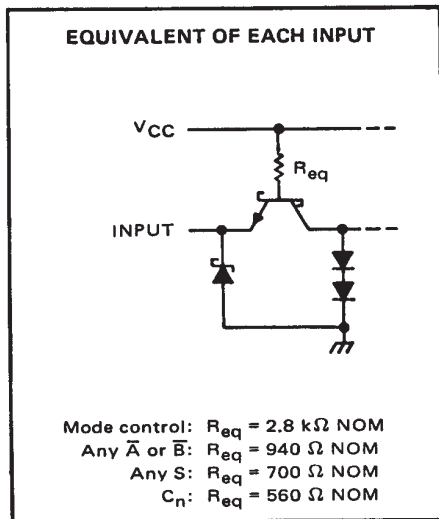
| PARAMETER† | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------|----------------------------|---------------|---|------|------|-----|------|
| t_{PLH} | C_n | C_{n+4} | | 7 | 10.5 | ns | |
| t_{PHL} | | | | 7 | 10.5 | | |
| t_{PLH} | Any \bar{A} or \bar{B} | C_{n+4} | $M = 0\text{ V}$, $S_0 = S_3 = 4.5\text{ V}$, $S_1 = S_2 = 0\text{ V}$ (SUM mode) | 12.5 | 18.5 | ns | |
| t_{PHL} | | | | 12.5 | 18.5 | | |
| t_{PLH} | Any \bar{A} or \bar{B} | C_{n+4} | $M = 0\text{ V}$, $S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ (DIFF mode) | 15.5 | 23 | ns | |
| t_{PHL} | | | | 15.5 | 23 | | |
| t_{PLH} | C_n | Any \bar{F} | $M = 0\text{ V}$ (SUM or DIFF mode) | 7 | 12 | ns | |
| t_{PHL} | | | | 7 | 12 | | |
| t_{PLH} | Any \bar{A} or \bar{B} | \bar{G} | $M = 0\text{ V}$, $S_0 = S_3 = 4.5\text{ V}$, $S_1 = S_2 = 0\text{ V}$ (SUM mode) | 8 | 12 | ns | |
| t_{PHL} | | | | 7.5 | 12 | | |
| t_{PLH} | Any \bar{A} or \bar{B} | \bar{G} | $M = 0\text{ V}$, $S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ (DIFF mode) | 10.5 | 15 | ns | |
| t_{PHL} | | | | 10.5 | 15 | | |
| t_{PLH} | Any \bar{A} or \bar{B} | \bar{P} | $M = 0\text{ V}$, $S_0 = S_3 = 4.5\text{ V}$, $S_1 = S_2 = 0\text{ V}$ (SUM mode) | 7.5 | 12 | ns | |
| t_{PHL} | | | | 7.5 | 12 | | |
| t_{PLH} | Any \bar{A} or \bar{B} | \bar{P} | $M = 0\text{ V}$, $S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ (DIFF mode) | 10.5 | 15 | ns | |
| t_{PHL} | | | | 10.5 | 15 | | |
| t_{PLH} | \bar{A}_i or \bar{B}_i | \bar{F}_i | $M = 0\text{ V}$, $S_0 = S_3 = 4.5\text{ V}$, $S_1 = S_2 = 0\text{ V}$ (SUM mode) | 11 | 16.5 | ns | |
| t_{PHL} | | | | 11 | 16.5 | | |
| t_{PLH} | \bar{A}_i or \bar{B}_i | F_i | $M = 0\text{ V}$, $S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ (DIFF mode) | 14 | 20 | ns | |
| t_{PHL} | | | | 14 | 22 | | |
| t_{PLH} | \bar{A}_i or \bar{B}_i | \bar{F}_i | $M = 4.5\text{ V}$ (logic mode) | 14 | 20 | ns | |
| t_{PHL} | | | | 14 | 22 | | |
| t_{PLH} | Any \bar{A} or \bar{B} | $A = B$ | $M = 0\text{ V}$, $S_0 = S_3 = 0\text{ V}$, $S_1 = S_2 = 4.5\text{ V}$ (DIFF mode) | 15 | 23 | ns | |
| t_{PHL} | | | | 20 | 30 | | |

† t_{PLH} = propagation delay time, low-to-high-level output

t_{PHL} = propagation delay time, high-to-low-level output

NOTE 4: Load circuits and voltage waveforms are shown in Section 1. Refer to Parameter Measurement Information page for test conditions.

schematics of inputs and outputs



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PARAMETER MEASUREMENT INFORMATION

SUM MODE TEST TABLE
 FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

| PARAMETER | INPUT UNDER TEST | OTHER INPUT SAME BIT | | OTHER DATA INPUTS | | OUTPUT UNDER TEST | OUTPUT WAVEFORM (See Note 4) |
|------------------|------------------|----------------------|-------------|-----------------------------------|---|----------------------------|------------------------------|
| | | APPLY 4.5 V | APPLY GND | APPLY 4.5 V | APPLY GND | | |
| ^t PLH | \bar{A}_i | \bar{B}_i | None | Remaining \bar{A} and \bar{B} | C_n | \bar{F}_i | In-Phase |
| ^t PHL | \bar{A}_i | \bar{B}_i | None | Remaining \bar{A} and \bar{B} | C_n | \bar{F}_i | In-Phase |
| ^t PLH | \bar{B}_i | \bar{A}_i | None | Remaining \bar{A} and \bar{B} | C_n | \bar{F}_i | In-Phase |
| ^t PHL | \bar{B}_i | \bar{A}_i | None | Remaining \bar{A} and \bar{B} | C_n | \bar{F}_i | In-Phase |
| ^t PLH | \bar{A}_i | \bar{B}_i | None | None | Remaining \bar{A} and \bar{B} , C_n | \bar{P} | In-Phase |
| ^t PHL | \bar{A}_i | \bar{B}_i | None | None | Remaining \bar{A} and \bar{B} , C_n | \bar{P} | In-Phase |
| ^t PLH | \bar{B}_i | \bar{A}_i | None | None | Remaining \bar{A} and \bar{B} , C_n | \bar{P} | In-Phase |
| ^t PHL | \bar{B}_i | \bar{A}_i | None | None | Remaining \bar{A} and \bar{B} , C_n | \bar{P} | In-Phase |
| ^t PLH | \bar{A}_i | None | \bar{B}_i | Remaining \bar{B} | Remaining \bar{A} , C_n | \bar{G} | In-Phase |
| ^t PHL | \bar{A}_i | None | \bar{B}_i | Remaining \bar{B} | Remaining \bar{A} , C_n | \bar{G} | In-Phase |
| ^t PLH | \bar{B}_i | None | \bar{A}_i | Remaining \bar{B} | Remaining \bar{A} , C_n | \bar{G} | In-Phase |
| ^t PHL | \bar{B}_i | None | \bar{A}_i | Remaining \bar{B} | Remaining \bar{A} , C_n | \bar{G} | In-Phase |
| ^t PLH | C_n | None | None | All \bar{A} | All \bar{B} | Any \bar{F} or C_{n+4} | In-Phase |
| ^t PHL | C_n | None | None | All \bar{A} | All \bar{B} | Any \bar{F} or C_{n+4} | In-Phase |
| ^t PLH | \bar{A}_i | None | \bar{B}_i | Remaining \bar{B} | Remaining \bar{A} , C_n | C_{n+4} | Out-of-Phase |
| ^t PHL | \bar{A}_i | None | \bar{B}_i | Remaining \bar{B} | Remaining \bar{A} , C_n | C_{n+4} | Out-of-Phase |
| ^t PLH | \bar{B}_i | None | \bar{A}_i | Remaining \bar{B} | Remaining \bar{A} , C_n | C_{n+4} | Out-of-Phase |
| ^t PHL | \bar{B}_i | None | \bar{A}_i | Remaining \bar{B} | Remaining \bar{A} , C_n | C_{n+4} | Out-of-Phase |

DIFF MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

| PARAMETER | INPUT UNDER TEST | OTHER INPUT SAME BIT | | OTHER DATA INPUTS | | OUTPUT UNDER TEST | OUTPUT WAVEFORM (See Note 4) |
|------------------|------------------|----------------------|-------------|-----------------------------|---|----------------------------|------------------------------|
| | | APPLY 4.5 V | APPLY GND | APPLY 4.5 V | APPLY GND | | |
| ^t PLH | \bar{A}_i | None | \bar{B}_i | Remaining \bar{A} | Remaining \bar{B} , C_n | \bar{F}_i | In-Phase |
| ^t PHL | \bar{A}_i | None | \bar{B}_i | Remaining \bar{A} | Remaining \bar{B} , C_n | \bar{F}_i | In-Phase |
| ^t PLH | \bar{B}_i | \bar{A}_i | None | Remaining \bar{A} | Remaining \bar{B} , C_n | \bar{F}_i | Out-of-Phase |
| ^t PHL | \bar{B}_i | \bar{A}_i | None | Remaining \bar{A} | Remaining \bar{B} , C_n | \bar{F}_i | Out-of-Phase |
| ^t PLH | \bar{A}_i | None | \bar{B}_i | None | Remaining \bar{A} and \bar{B} , C_n | \bar{P} | In-Phase |
| ^t PHL | \bar{A}_i | None | \bar{B}_i | None | Remaining \bar{A} and \bar{B} , C_n | \bar{P} | In-Phase |
| ^t PLH | \bar{B}_i | \bar{A}_i | None | None | Remaining \bar{A} and \bar{B} , C_n | \bar{P} | Out-of-Phase |
| ^t PHL | \bar{B}_i | \bar{A}_i | None | None | Remaining \bar{A} and \bar{B} , C_n | \bar{P} | Out-of-Phase |
| ^t PLH | \bar{A}_i | \bar{B}_i | None | None | Remaining \bar{A} and \bar{B} , C_n | \bar{G} | In-Phase |
| ^t PHL | \bar{A}_i | \bar{B}_i | None | None | Remaining \bar{A} and \bar{B} , C_n | \bar{G} | In-Phase |
| ^t PLH | \bar{B}_i | None | \bar{A}_i | None | Remaining \bar{A} and \bar{B} , C_n | \bar{G} | Out-of-Phase |
| ^t PHL | \bar{B}_i | None | \bar{A}_i | None | Remaining \bar{A} and \bar{B} , C_n | \bar{G} | Out-of-Phase |
| ^t PLH | \bar{A}_i | None | \bar{B}_i | Remaining \bar{A} | Remaining \bar{B} , C_n | A = B | In-Phase |
| ^t PHL | \bar{A}_i | None | \bar{B}_i | Remaining \bar{A} | Remaining \bar{B} , C_n | A = B | In-Phase |
| ^t PLH | \bar{B}_i | \bar{A}_i | None | Remaining \bar{A} | Remaining \bar{B} , C_n | A = B | Out-of-Phase |
| ^t PHL | \bar{B}_i | \bar{A}_i | None | Remaining \bar{A} | Remaining \bar{B} , C_n | A = B | Out-of-Phase |
| ^t PLH | C_n | None | None | All \bar{A} and \bar{B} | None | C_{n+4} or any \bar{F} | In-Phase |
| ^t PHL | C_n | None | None | All \bar{A} and \bar{B} | None | C_{n+4} or any \bar{F} | In-Phase |
| ^t PLH | \bar{A}_i | \bar{B}_i | None | None | Remaining \bar{A} , \bar{B} , C_n | C_{n+4} | Out-of-Phase |
| ^t PHL | \bar{A}_i | \bar{B}_i | None | None | Remaining \bar{A} , \bar{B} , C_n | C_{n+4} | Out-of-Phase |
| ^t PLH | \bar{B}_i | None | \bar{A}_i | None | Remaining \bar{A} , \bar{B} , C_n | C_{n+4} | Out-of-Phase |
| ^t PHL | \bar{B}_i | None | \bar{A}_i | None | Remaining \bar{A} , \bar{B} , C_n | C_{n+4} | Out-of-Phase |

LOGIC MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

| PARAMETER | INPUT UNDER TEST | OTHER INPUT SAME BIT | | OTHER DATA INPUTS | | OUTPUT UNDER TEST | OUTPUT WAVEFORM (See Note 4) |
|------------------|------------------|----------------------|-----------|-------------------|---|-------------------|------------------------------|
| | | APPLY 4.5 V | APPLY GND | APPLY 4.5 V | APPLY GND | | |
| ^t PLH | \bar{A}_i | \bar{B}_i | None | None | Remaining \bar{A} and \bar{B} , C_n | \bar{F}_i | Out-of-Phase |
| ^t PHL | \bar{A}_i | \bar{B}_i | None | None | Remaining \bar{A} and \bar{B} , C_n | \bar{F}_i | Out-of-Phase |
| ^t PLH | \bar{B}_i | \bar{A}_i | None | None | Remaining \bar{A} and \bar{B} , C_n | \bar{F}_i | Out-of-Phase |
| ^t PHL | \bar{B}_i | \bar{A}_i | None | None | Remaining \bar{A} and \bar{B} , C_n | \bar{F}_i | Out-of-Phase |

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.



PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| JM38510/07801BJA | ACTIVE | CDIP | J | 24 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | JM38510/ 07801BJA | Samples |
| M38510/07801BJA | ACTIVE | CDIP | J | 24 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | JM38510/ 07801BJA | Samples |
| SN54LS181J | ACTIVE | CDIP | J | 24 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | SN54LS181J | Samples |
| SN54S181J | ACTIVE | CDIP | J | 24 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | SN54S181J | Samples |
| SN74LS181N3 | OBSOLETE | PDIP | N | 24 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74S181J | OBSOLETE | CDIP | J | 24 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74S181N | OBSOLETE | PDIP | N | 24 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SN74S181N3 | OBSOLETE | PDIP | N | 24 | | TBD | Call TI | Call TI | 0 to 70 | | |
| SNJ54LS181J | ACTIVE | CDIP | J | 24 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | SNJ54LS181J | Samples |
| SNJ54S181J | ACTIVE | CDIP | J | 24 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | SNJ54S181J | Samples |
| SNJ54S181W | ACTIVE | CFP | W | 24 | 1 | TBD | A42 | N / A for Pkg Type | -55 to 125 | SNJ54S181W | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54LS181, SN54S181, SN74LS181, SN74S181 :

● Catalog: [SN74LS181](#), [SN74S181](#)

● Military: [SN54LS181](#), [SN54S181](#)

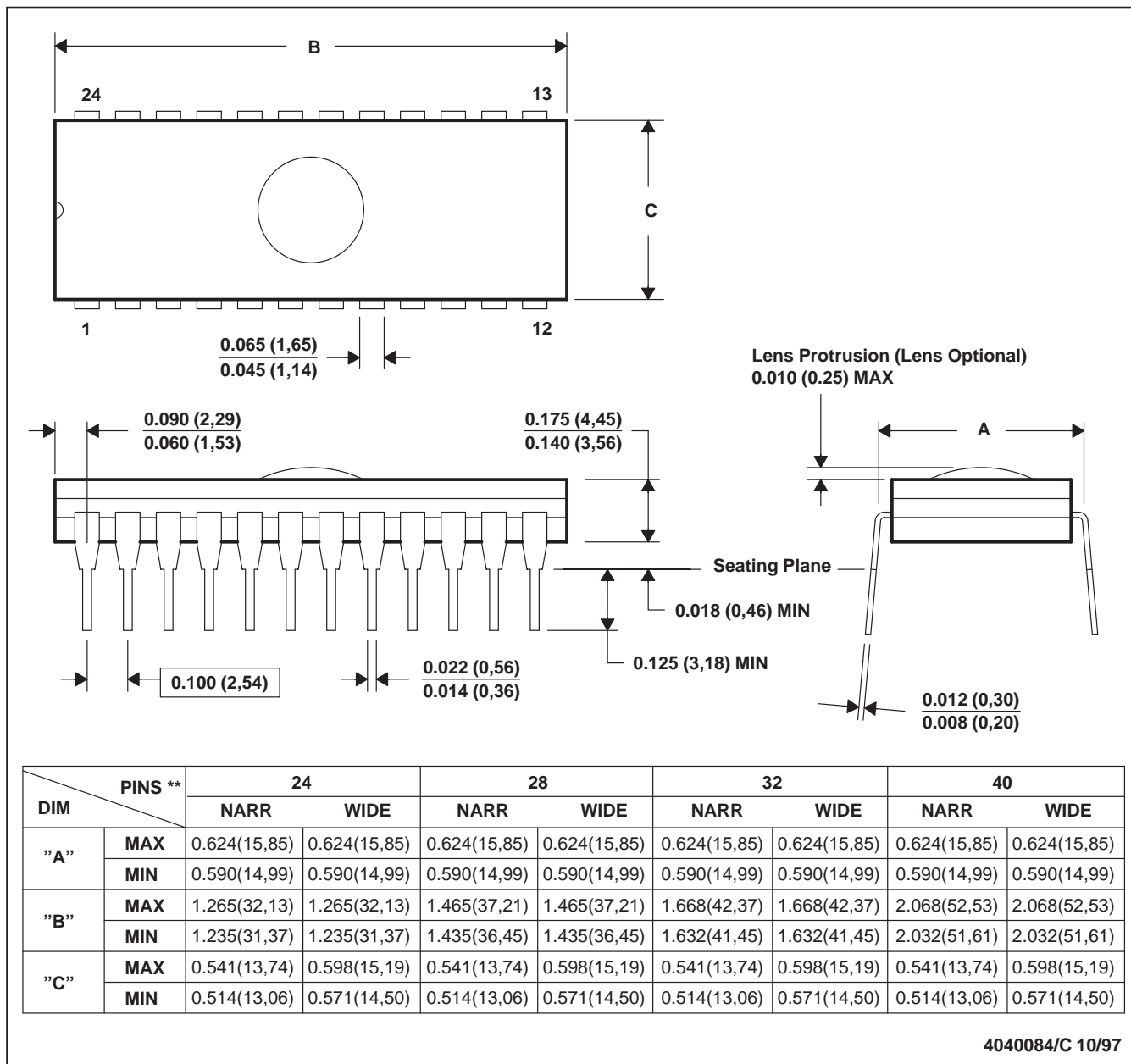
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

J (R-GDIP-T**)

CERAMIC DUAL-IN-LINE PACKAGE

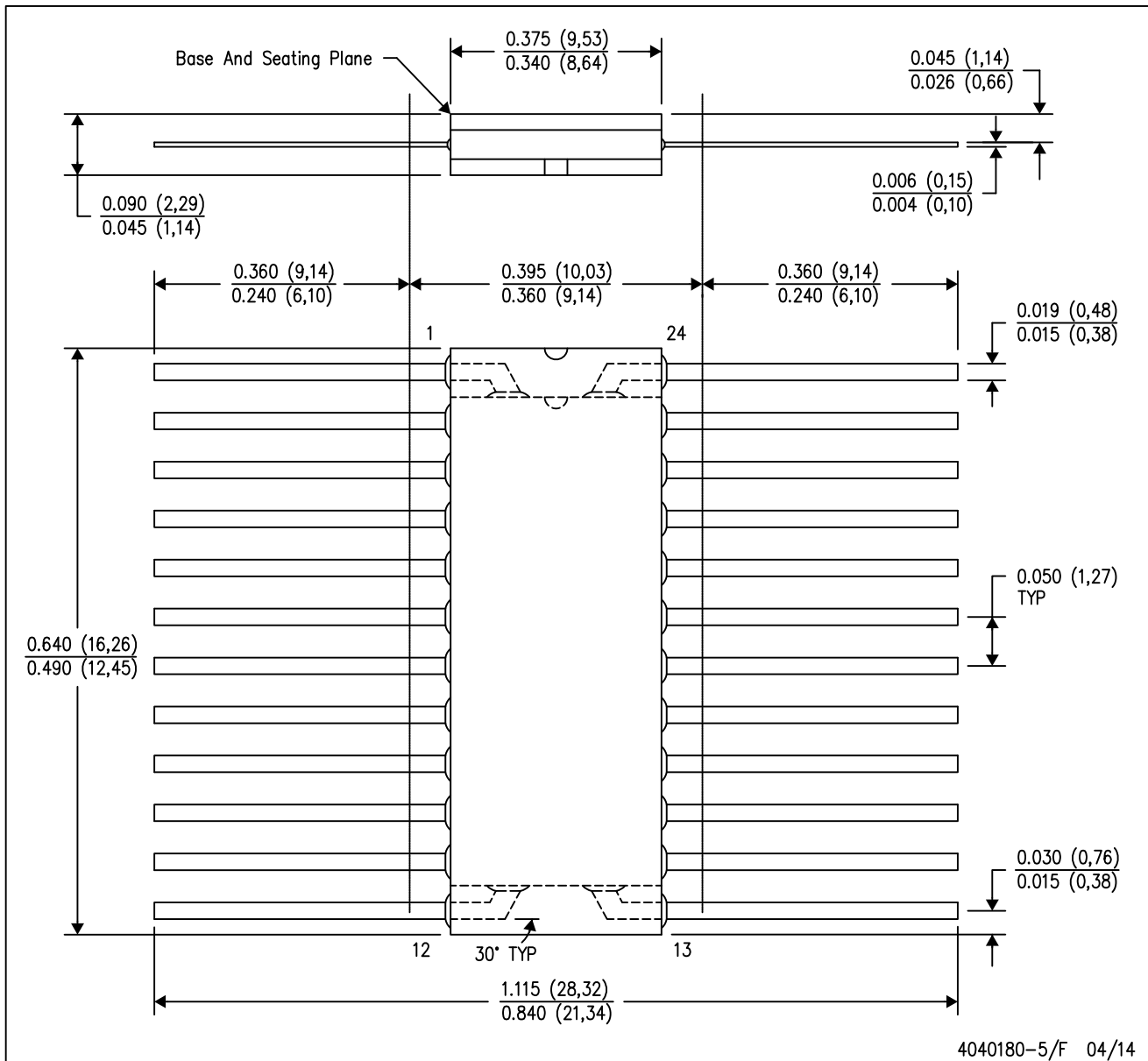
24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Window (lens) added to this group of packages (24-, 28-, 32-, 40-pin).
 D. This package can be hermetically sealed with a ceramic lid using glass frit.
 E. Index point is provided on cap for terminal identification.

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK

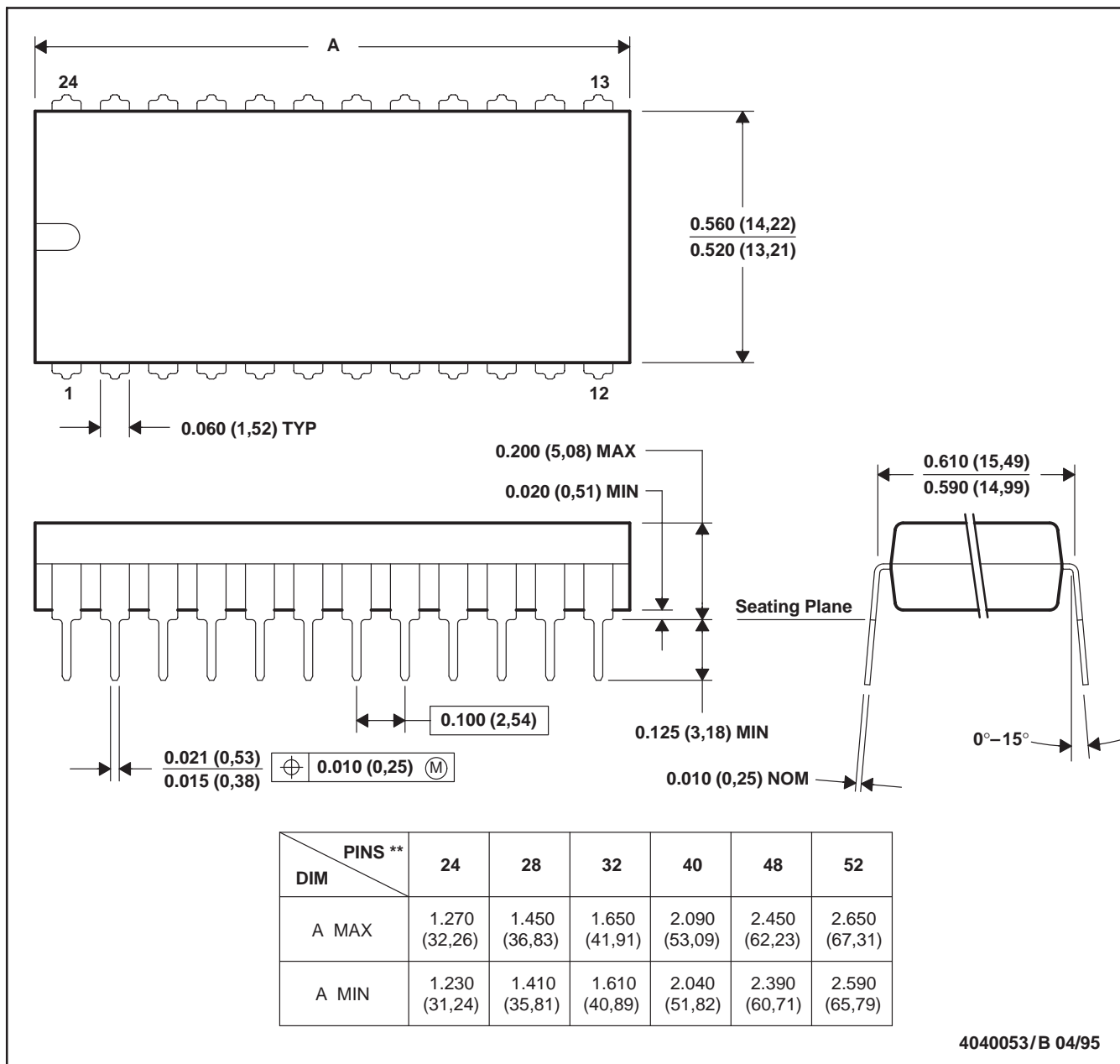


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

N (R-PDIP-T)**

PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-011
 D. Falls within JEDEC MS-015 (32 pin only)

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Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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