TEXAS INSTRUMENTS

LM78L05, LM78L09
LM78L12, LM78L15, LM78L62

SNVS754K – JANUARY 2000 – REVISED DECEMBER 2016

LM78Lxx 100-mA Fixed Output Linear Regulator

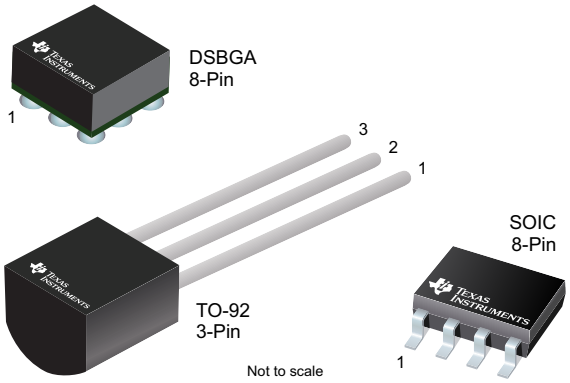
1 Features

- Input Voltage up to 30 V
- Output Voltage Tolerances of ±5% Over the Temperature Range
- Available Output Voltages: 5 V, 6.2 V, 8.2 V, 9 V, 12 V, and 15 V
- Output Current of 100 mA
- Output Transistor Safe Area Protection
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limit
- No External Components
- Available in Tiny DSBGA Package
- Available in 3-Pin TO-92 and 8-Pin SOIC Low Profile Packages

2 Applications

- Battery Chargers
- Portable Instrumentation
- LED Lighting
- Low Wattage Power Supplies

Package Options



3 Description

The LM78Lxx series of three terminal positive regulators is available with several fixed output voltages, making them useful in a wide range of applications. Used as a Zener-diode and resistor combination replacement, the LM78Lxx usually provides an effective output impedance improvement of two orders of magnitude and lower quiescent current. These regulators can provide local, on-card regulation, eliminating distribution problems associated with single-point regulation. The available voltages allow the LM78Lxx to be used in logic systems, instrumentation, HiFi, and other solid-state electronic equipment.

The LM78Lxx is available in the plastic TO-92 (LP) package, the SOIC (D) package, and a chip-sized package (8-Bump DSBGA) using TI's DSBGA package technology. With adequate heat sinking, the regulator can deliver 100-mA output current. Current limiting is included to limit the peak output current to a safe value. Safe area protection for the output transistors is provided to limit internal power dissipation. If internal power dissipation is too high for the heat sinking provided, the thermal shutdown circuit prevents the IC from overheating.

See *AN-1112 DSBGA Wafer Level Chip Scale Package* (SNVA009) for DSBGA Considerations. For more information on the TO-92 package, see *TO-92 Packing Options / Ordering Instructions* (SNOA072).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM78L05, LM78L09	DSBGA (8)	1.30 mm × 1.30 mm
LM78L05, LM78L12, LM78L15	SOIC (8)	3.90 mm × 4.90 mm
LM78L05, LM78L12, LM78L15, LM78L62	TO-92 (3)	3.70 mm × 4.70 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Fixed Output Regulator Circuit

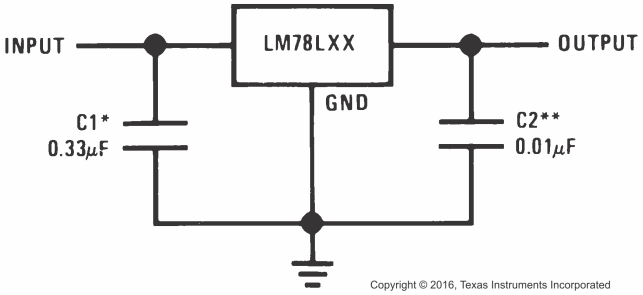


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (December 2013) to Revision K — **Page**

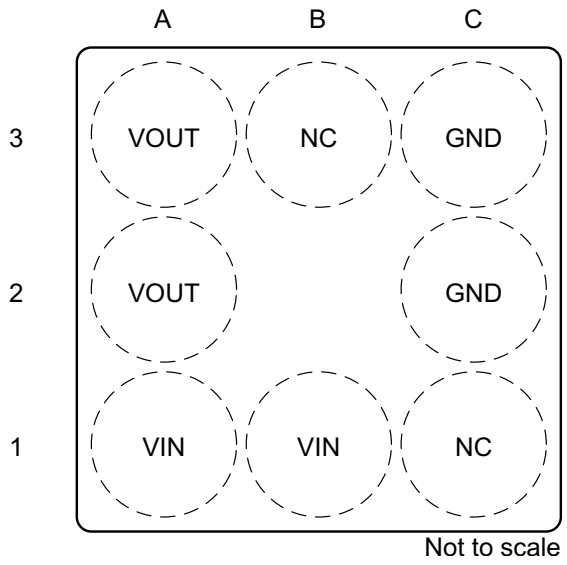
- Added *Applications* section, *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Recommended Operating Conditions* table, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Deleted LM78L82 from the data sheet ... 1
- Added *Thermal Information* table. ... 1
- Deleted Lead temperature (soldering) information ... 4
- Changed $R_{\theta JA}$ values for D (SOIC) From: 180 To: 128.8, LP (TO-92) from 230 to 158.7, and YPB (DSBGA) From: 230.9 To 108.4 ... 4
- Changed $R_{\theta JC}$ values for LP (TO-92) From: 60 To 75.2 ... 4

Changes from Revision I (April 2013) to Revision J — **Page**

- Added the AI suffix ... 5

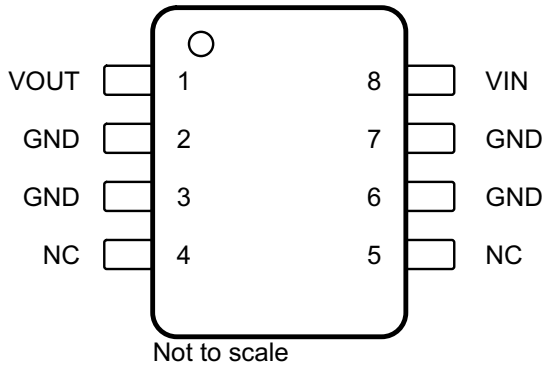
5 Pin Configuration and Functions

YPB Package
8-Pin DSBGA
Top View



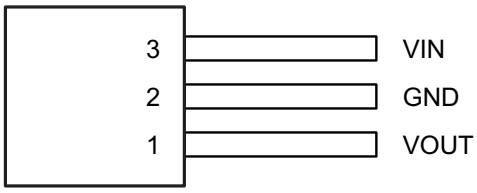
Not to scale

D Package
8-Pin SOIC
Top View



Not to scale

LP Package
3-Pin TO-92
Bottom View



Not to scale

Pin Functions

PIN				I/O	DESCRIPTION
NAME	DSBGA	SOIC	TO-92		
GND	C2, C3	2, 3, 6, 7	2	—	Ground
NC	B3, C1	4, 5	—	—	No connection
VIN	A1, B1	8	3	I	Input supply voltage pin
VOUT	A2, A3	1	1	O	Output voltage pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	MAX	UNIT
Input voltage			35	V
Power dissipation		Internally limited		
Operating junction temperature, T_J	LM78LxxACZ (TO-92)	0	125	°C
	LM78LxxACM (SOIC)	0	125	
	LM78LxxAIM (SOIC)	–40	125	
	LM78LxxITP (thin DSBGA)	–40	85	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM),(1)	±1000	V

(1) Human body model, 1.5 kΩ in series with 100 pF.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Input voltage				30	V
	Continuous output current				100	mA
T_J	Junction temperature	LM78LxxACZ (TO-92)	0		125	°C
		LM78LxxACM (SOIC)	0		125	
		LM78LxxAIM (SOIC)	–40		125	
		LM78LxxITP (DSBGA)	–40		85	

6.4 Thermal Information

THERMAL METRIC(1)		LM78Lxx			UNIT
		D (SOIC)	LP (TO-92)	YPB (DSBGA)	
		8 PINS	3 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	128.8	158.7	108.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	76	75.2	1.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.3	n/a	31.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	26.3	30.2	4.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	68.8	138.2	31.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics — LM78L05

Typical values apply for T_J = 25°C, Minimum and Maximum limits apply for the entire operating temperature range of the package[1][2], I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, V_{IN} = 10 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	T_J = 25°C	4.8	5	5.2	V
		V_{IN} = 7 V to 20 V, I_O = 1 mA to 40 mA[3]	4.75		5.25	
		I_O = 1 mA to 70 mA[3]	4.75		5.25	
ΔV_O	Line regulation	V_{IN} = 7 V to 20 V, T_J = 25°C		18	75	mV
		V_{IN} = 8 V to 20 V, T_J = 25°C		10	54	
	Load regulation	I_O = 1 mA to 100 mA, T_J = 25°C		20	60	
		I_O = 1 mA to 40 mA, T_J = 25°C		5	30	
I_Q	Quiescent current	T_J = 25°C		3	5	mA
ΔI_Q	Quiescent current change	V_{IN} = 8 V to 20 V			1	mA
		I_O = 1 mA to 40 mA			0.1	
V_n	Output noise voltage	f = 10 Hz to 100 kHz[4]		40		µV
$\Delta V_{IN}/\Delta V_O$	Ripple rejection	f = 120 Hz, V_{IN} = 8 V to 16 V, T_J = 25°C	47	62		dB
I_{PK}	Peak output current			140		mA
$\Delta V_O/\Delta T$	Average output voltage temperature coefficient	I_O = 5 mA		–0.65		mV/°C
$V_{IN(MIN)}$	Minimum value of input voltage required to maintain line regulation	T_J = 25°C		6.7	7	V

(1) For the operating ranges of each package, see *Absolute Maximum Ratings*.
(2) Limits are ensured by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods.
(3) Power dissipation ≤ 0.75 W.
(4) Recommended minimum load capacitance of 0.01 µF to limit high-frequency noise.

6.6 Electrical Characteristics — LM78L09

Typical values apply for T_J = 25°C, Minimum and Maximum limits apply for the entire operating temperature range of the package[1][2], I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, V_{IN} = 15 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	T_J = 25°C	8.64	9	9.36	V
		V_{IN} = 11.5 V to 24 V, I_O = 1 mA to 40 mA[3]	8.55		9.45	
		I_O = 1 mA to 70 mA[3]	8.55		9.45	
ΔV_O	Line regulation	V_{IN} = 11.5 V to 24 V, T_J = 25°C		100	200	mV
		V_{IN} = 13 V to 24 V, T_J = 25°C		90	150	
	Load regulation	I_O = 1 mA to 100 mA, T_J = 25°C		20	90	
		I_O = 1 mA to 40 mA, T_J = 25°C		10	45	
I_Q	Quiescent current	T_J = 25°C		2	5.5	mA
ΔI_Q	Quiescent current change	V_{IN} = 11.5 V to 24 V			1.5	mA
		I_O = 1 mA to 40 mA			0.1	
V_n	Output noise voltage			70		µV
$\Delta V_{IN}/\Delta V_O$	Ripple rejection	f = 120 Hz, V_{IN} = 15 V to 25 V, T_J = 25°C	38	44		dB
I_{PK}	Peak output current			140		mA
$\Delta V_O/\Delta T$	Average output voltage temperature coefficient	I_O = 5 mA		–0.9		mV/°C
$V_{IN(MIN)}$	Minimum value of input voltage required to maintain line regulation			10.7		V

(1) For the operating ranges of each package, see *Absolute Maximum Ratings*.
(2) Limits are ensured by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods.
(3) Power dissipation ≤ 0.75 W.

6.7 Electrical Characteristics — LM78L12

Typical values apply for T_J = 25°C, Minimum and Maximum limits apply for the entire operating temperature range of the package[1][2], I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, V_{IN} = 19 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	T_J = 25°C	11.5	12	12.5	V
		V_{IN} = 14.5 V to 27 V, I_O = 1 mA to 40 mA[3]	11.4		12.6	
		I_O = 1 mA to 70 mA[3]	11.4		12.6	
ΔV_O	Line regulation	V_{IN} = 14.5 V to 27 V, T_J = 25°C		30	180	mV
		V_{IN} = 16 V to 27 V, T_J = 25°C		20	110	
	Load regulation	I_O = 1 mA to 100 mA, T_J = 25°C		30	100	
		I_O = 1 mA to 40 mA, T_J = 25°C		10	50	
I_Q	Quiescent current	T_J = 25°C		3	5	mA
ΔI_Q	Quiescent current change	V_{IN} = 16 V to 27 V			1	mA
		I_O = 1 mA to 40 mA			0.1	
V_n	Output noise voltage			80		µV
$\Delta V_{IN}/\Delta V_O$	Ripple rejection	f = 120 Hz, V_{IN} = 15 V to 25 V, T_J = 25°C	40	54		dB
I_{PK}	Peak output current			140		mA
$\Delta V_O/\Delta T$	Average output voltage temperature coefficient	I_O = 5 mA		–1		mV/°C
$V_{IN(MIN)}$	Minimum value of input voltage required to maintain line regulation	T_J = 25°C		13.7	14.5	V

(1) For the operating ranges of each package, see *Absolute Maximum Ratings*.
(2) Limits are ensured by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods.
(3) Power dissipation ≤ 0.75 W.

6.8 Electrical Characteristics — LM78L15

Typical values apply for T_J = 25°C, Minimum and Maximum limits apply for the entire operating temperature range of the package[1][2], I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, V_{IN} = 23 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	T_J = 25°C	14.4	15	15.6	V
		V_{IN} = 17.5 V to 30 V, I_O = 1 mA to 40 mA[3]	14.25		15.75	
		I_O = 1 mA to 70 mA[3]	14.25		15.75	
ΔV_O	Line regulation	V_{IN} = 17.5 V to 30 V, T_J = 25°C		37	250	mV
		V_{IN} = 20 V to 30 V, T_J = 25°C		25	140	
	Load regulation	I_O = 1 mA to 100 mA, T_J = 25°C		35	150	
		I_O = 1 mA to 40 mA, T_J = 25°C		12	75	
I_Q	Quiescent current	T_J = 25°C		3	5	mA
ΔI_Q	Quiescent current change	V_{IN} =20 V to 30 V			1	mA
		I_O = 1 mA to 40 mA			0.1	
V_n	Output noise voltage			90		µV
$\Delta V_{IN}/\Delta V_O$	Ripple rejection	f = 120 Hz, V_{IN} = 18.5 V to 28.5 V, T_J = 25°C	37	51		dB
I_{PK}	Peak output current			140		mA
$\Delta V_O/\Delta T$	Average output voltage temperature coefficient	I_O = 5 mA		–1.3		mV/°C
$V_{IN(MIN)}$	Minimum value of input voltage required to maintain line regulation	T_J = 25°C		16.7	17.5	V

(1) For the operating ranges of each package, see *Absolute Maximum Ratings*.
(2) Limits are ensured by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods.
(3) Power dissipation ≤ 0.75 W.

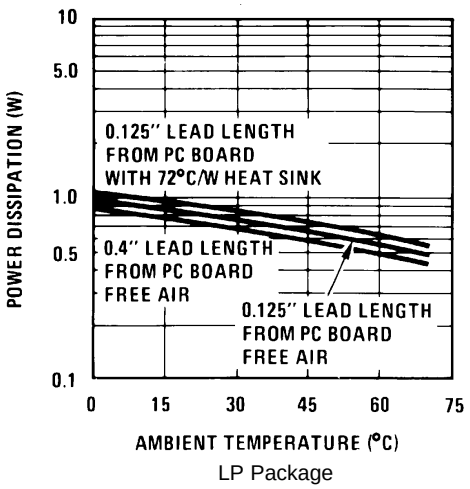
6.9 Electrical Characteristics — LM78L62

Typical values apply for T_J = 25°C, Minimum and Maximum limits apply for the entire operating temperature range of the package[1][2], I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, V_{IN} = 12 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_O	Output voltage	T_J = 25°C	5.95	6.2	6.45	V
		V_{IN} = 8.5 V to 20 V, I_O = 1 mA to 40 mA[3]	5.9		6.5	
		I_O = 1 mA to 70 mA[3]	5.9		6.5	
ΔV_O	Line regulation	V_{IN} = 8.5 V to 20 V, T_J = 25°C		65	175	mV
		V_{IN} = 9 V to 20 V, T_J = 25°C		55	125	
	Load regulation	I_O = 1 mA to 100 mA, T_J = 25°C		13	80	
		I_O = 1 mA to 40 mA, T_J = 25°C		6	40	
I_Q	Quiescent current	T_J = 25°C		2	5.5	mA
ΔI_Q	Quiescent current change	V_{IN} = 8 V to 20 V			1.5	mA
		I_O = 1 mA to 40 mA			0.1	
V_n	Output noise voltage	f = 10 Hz to 100 kHz[4]		50		µV
$\Delta V_{IN}/\Delta V_O$	Ripple rejection	f = 120 Hz, V_{IN} = 10 V to 20 V, T_J = 25°C	40	46		dB
I_{PK}	Peak output current			140		mA
$\Delta V_O/\Delta T$	Average output voltage temperature coefficient	I_O = 5 mA		–0.75		mV/°C
$V_{IN(MIN)}$	Minimum value of input voltage required to maintain line regulation			7.9		V

(1) For the operating ranges of each package, see *Absolute Maximum Ratings*.
(2) Limits are ensured by production testing or correlation techniques using standard Statistical Quality Control (SQC) methods.
(3) Power dissipation ≤ 0.75 W.
(4) Recommended minimum load capacitance of 0.01 µF to limit high-frequency noise.

6.10 Typical Characteristics



LP Package

Figure 1. Maximum Average Power Dissipation

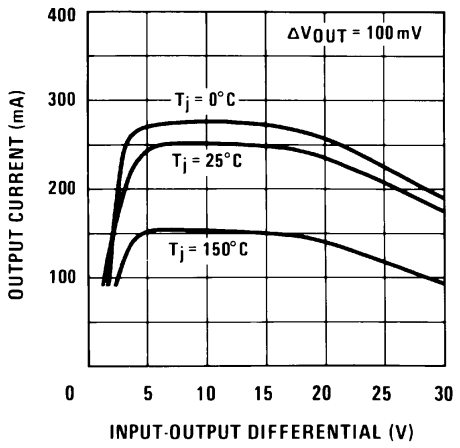


Figure 2. Peak Output Current

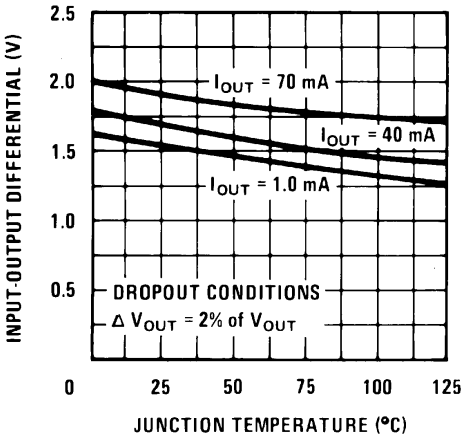


Figure 3. Dropout Voltage

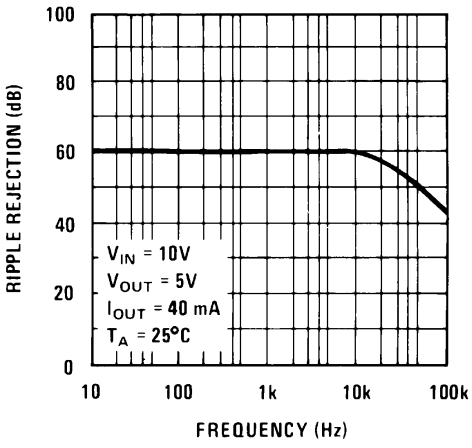


Figure 4. Ripple Rejection

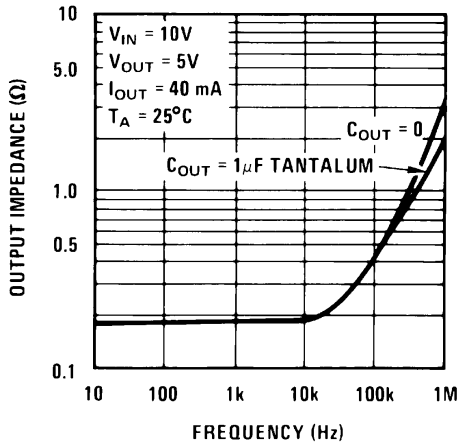


Figure 5. Output Impedance

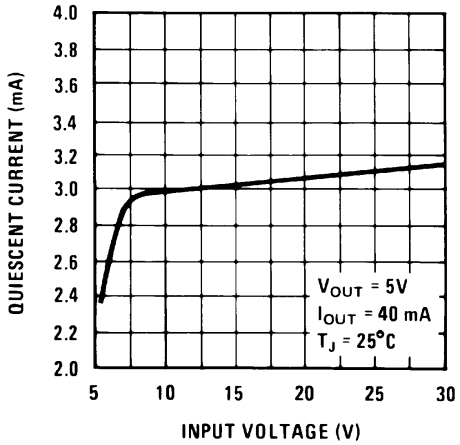


Figure 6. Quiescent Current

Typical Characteristics (continued)

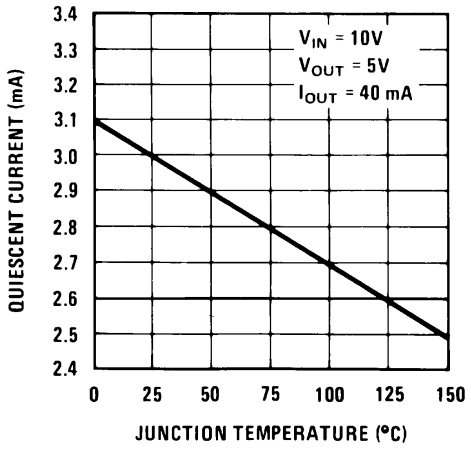


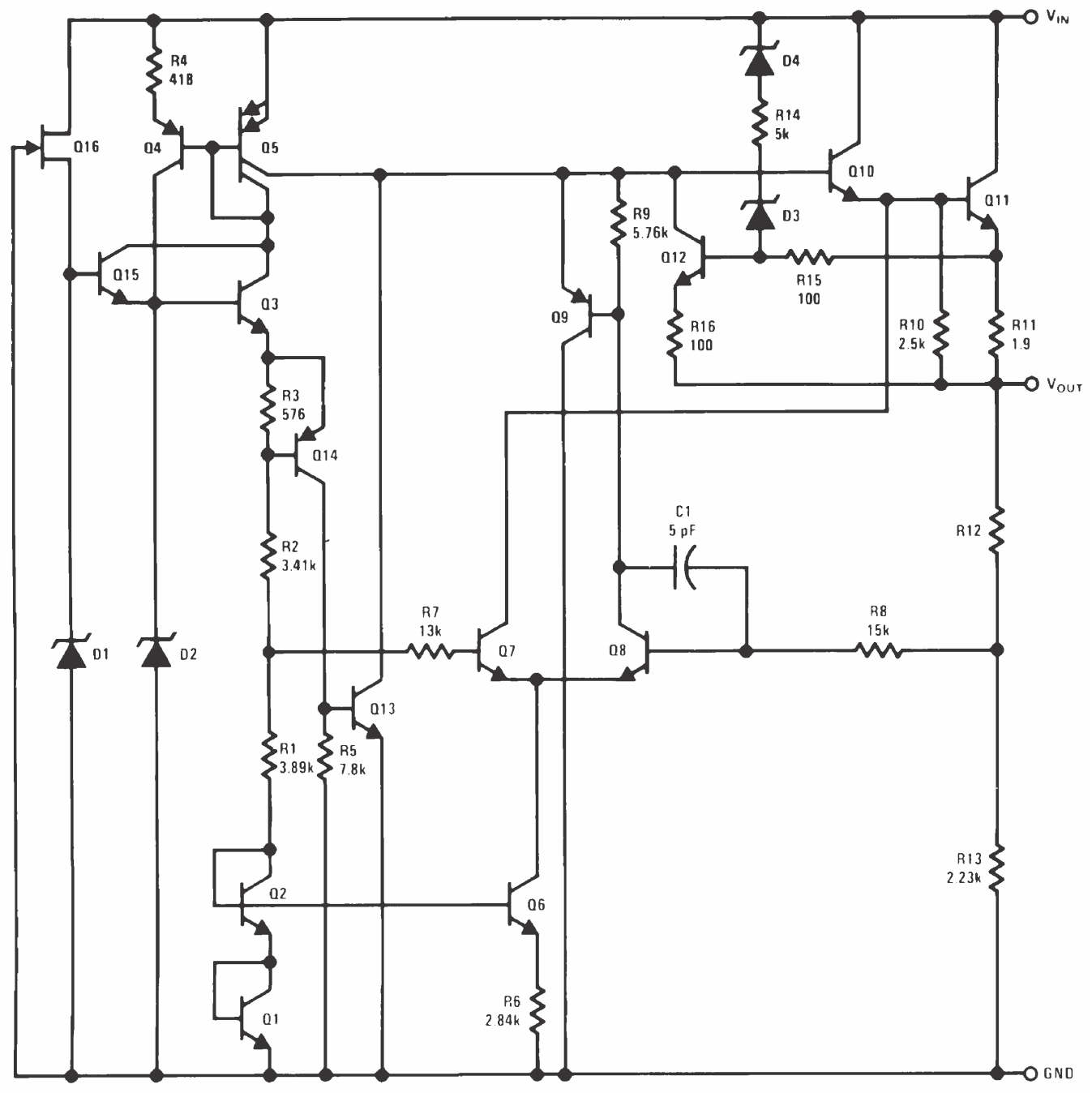
Figure 7. Quiescent Current

7 Detailed Description

7.1 Overview

The LM78Lxx series of positive regulators is available in the following fixed output voltages: 5 V, 6.2 V, 8.2 V, 9 V, 12 V, and 15 V. The regulator can be configured to an adjustable output by connecting the GND pin to the center of a resistive voltage divider as shown in Figure 10. In this configuration, the fixed output voltage acts as the reference voltage across R1 allowing the output to be adjusted by changing the resistor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Load Regulation

These devices regulate the voltage between the VOUT and GND pins, and can be made adjustable by using a resistive voltage divider. The output voltage tolerance is ±5% over temperature.

7.3.2 Protection

The LM78Lxx series of regulators has internal thermal overload protection that automatically shuts off the device if the operating temperature becomes too high. There is also internal short-circuit current limit and output transistor safe area protection that shuts down the device if the output current becomes too high.

7.4 Device Functional Modes

7.4.1 Normal Operation

The VOUT pin sources current necessary to set the voltage on VOUT at a fixed voltage above the GND pin. See *Specifications* for V_O of each device.

7.4.2 Shutdown

The device automatically shuts down if the output current or its internal temperature becomes too high.

8 Application and Implementation

NOTE

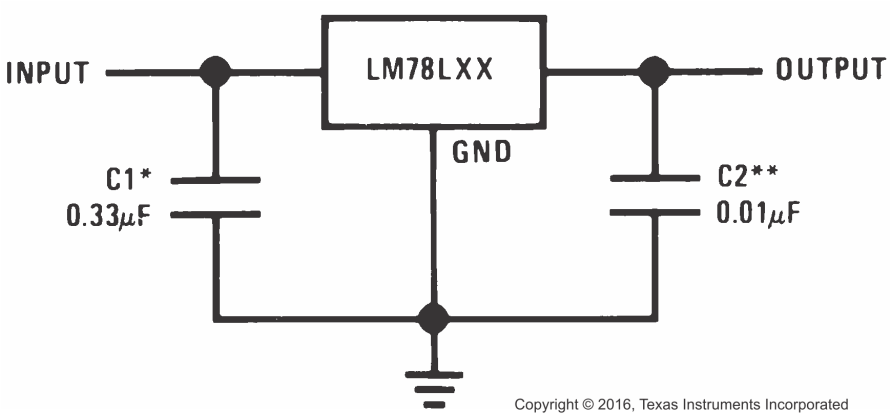
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

These devices are versatile and high-performance regulators with a wide temperature range and tight line and load regulation. An input capacitor is required if the regulator is placed more than 3 inches from the power supply filter. TI recommends a minimum load capacitance of 0.01 µF to limit high frequency.

8.2 Typical Applications

8.2.1 Fixed Output Regulator



*Required if the regulator is located more than 3 inches from the power supply filter.

**Recommended minimum load capacitance of 0.01 µF to limit high-frequency noise.

Figure 8. Fixed Output Regulator Circuit

8.2.1.1 Design Requirements

The device component count is very minimal. No external components are usually required. However, TI recommends input or output capacitors depending on the distance between the device and the power supply and if extra filtering is needed at the output.

The output voltage is set based on the selection of the two resistors (R1 and R2), as shown in Figure 14.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Input Capacitor

An input capacitor is required if the regulator is placed more than 3 inches from the power supply filter. A 0.33-µF capacitor on the input is suitable for most applications.

8.2.1.2.2 Output Capacitor

TI recommends a minimum load capacitance of 0.01 µF to limit high-frequency noise.

Typical Applications (continued)

8.2.1.3 Application Curve

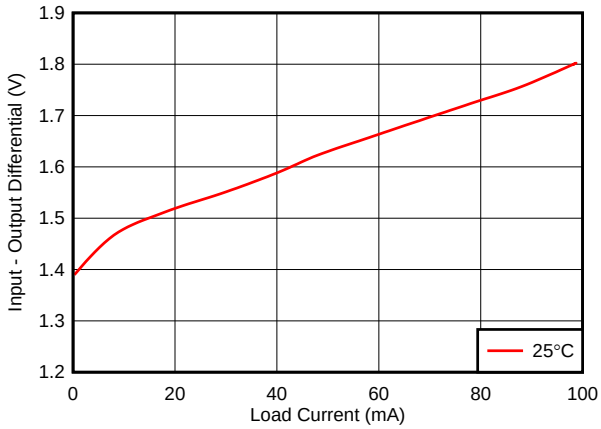
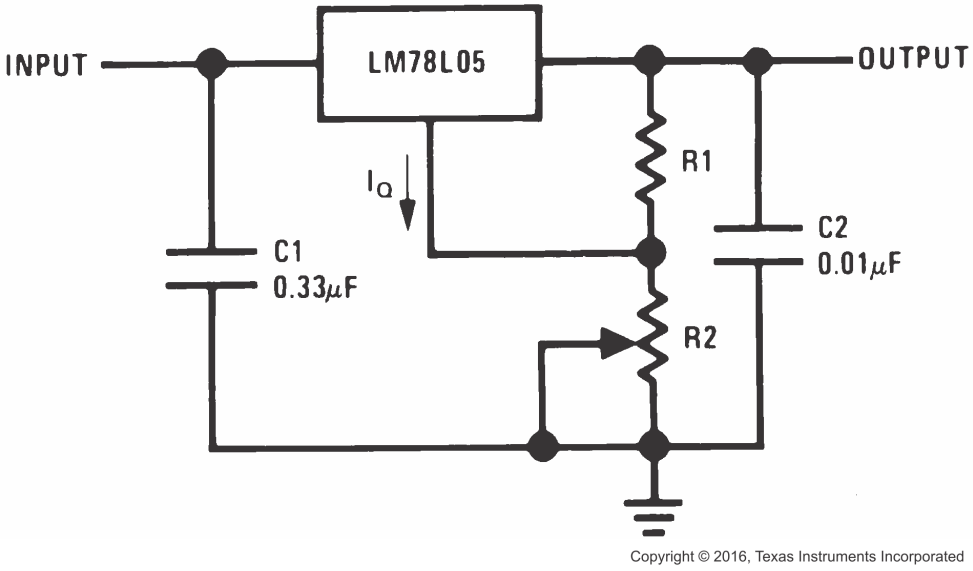


Figure 9. LM78Lxx Dropout

8.2.2 Other Application Circuits

Figure 10 to Figure 14 show application circuit examples using the LM78Lxx devices. Customers must fully validate and test these circuits before implementing a design based on these examples. Unless otherwise noted, the design procedures in *Fixed Output Regulator* are applicable to these designs.



$V_O = 5\ V + (5\ V / R1 + I_Q) \times R2$*

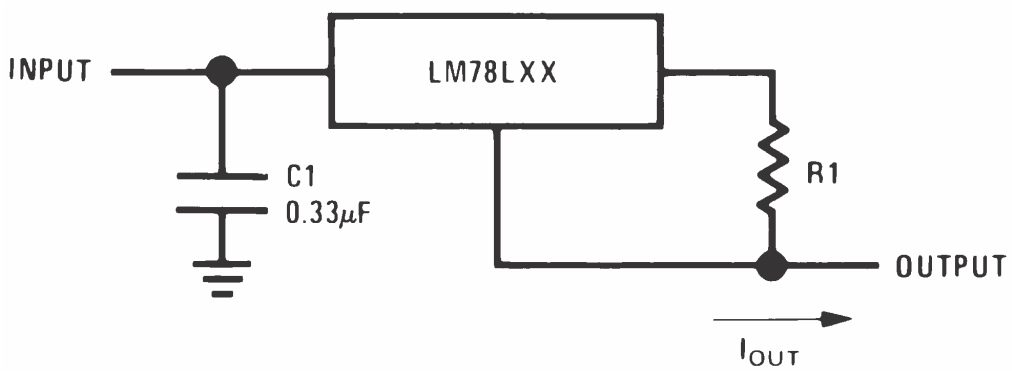
* The 5 V represents the fixed output voltage of the LM78L05. If using one of the other LM78Lxx devices, use that fixed output voltage value when calculating V_O.

$I_Q < 5\ V / (3 \times R1)$

Load regulation (L_R) of LM78L05 ≈ (R1 + R2) / R1

Figure 10. Adjustable Output Regulator Circuit

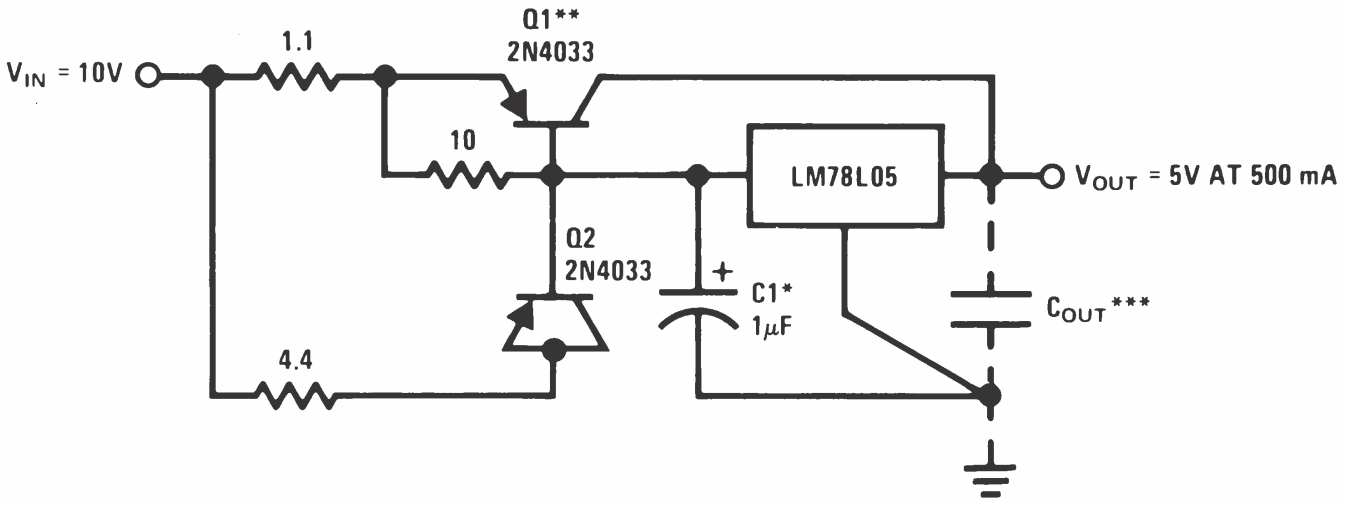
Typical Applications (continued)



$I_{OUT} = (V_O / R1) + I_Q$

I_Q = 1.5 mA over line and load changes

Figure 11. Current Regulator Circuit



*Solid tantalum

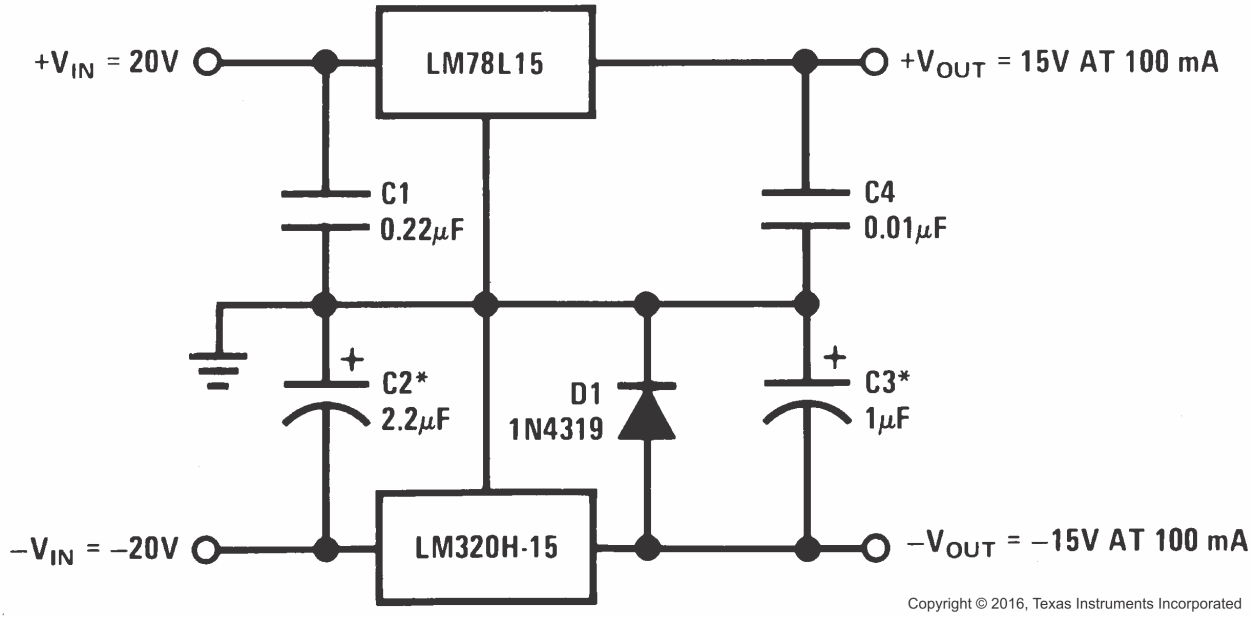
**Heat sink Q1

***Optional: Improves ripple rejection and transient response.

Load Regulation = 0.6%, I_L = 0 mA to 250 mA pulsed with t_{ON} = 50 ms.

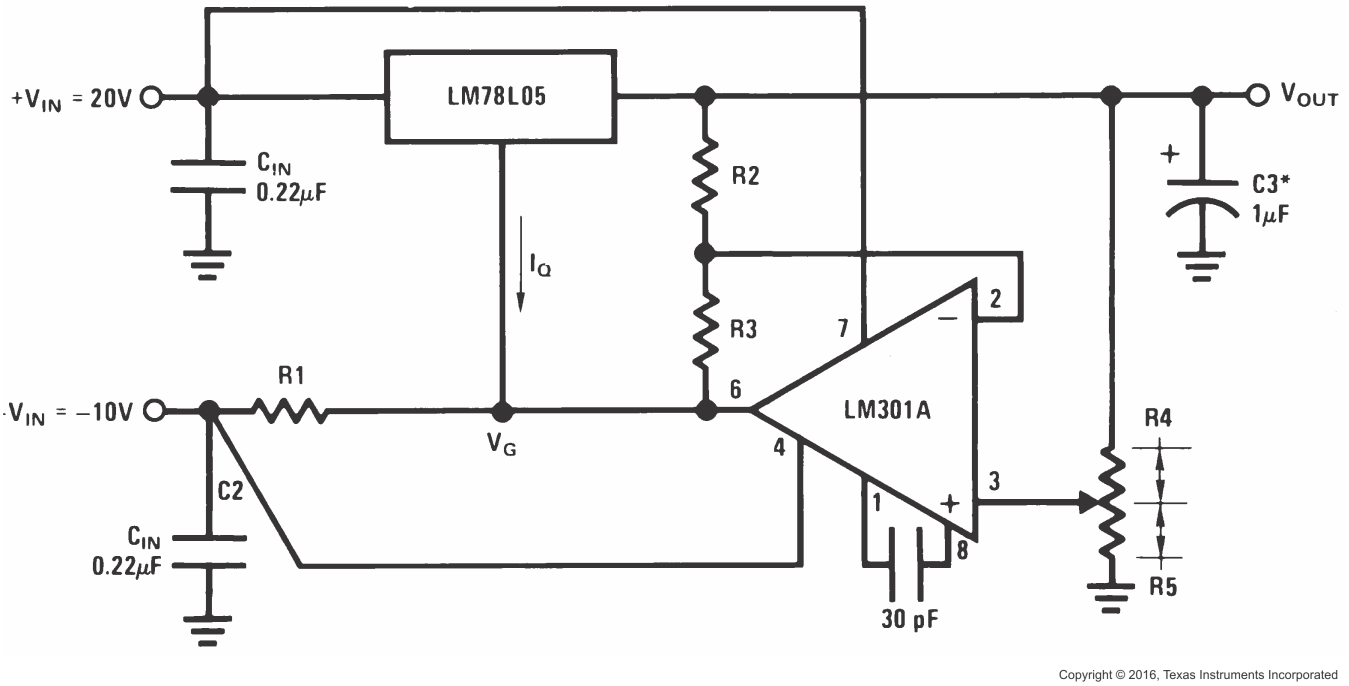
Figure 12. 5-V, 500-mA Regulator With Short-Circuit Protection Circuit

Typical Applications (continued)



*Solid tantalum

Figure 13. ±15-V, 100-mA Dual Power Supply Circuit



*Solid tantalum

$V_O = V_G + 5$ V, R1 = $(-V_{IN} / I_{Q(LM78L05)})$

$V_O = 5$ V (R2 / R4) for (R2 + R3) = (R4 + R5)

A 0.5-V output will correspond to (R2 / R4) = 0.1, (R3 / R4) = 0.9

Figure 14. Variable Output Regulator Circuit (0.5 V to 18 V)

9 Power Supply Recommendations

The linear regulator input supply must be well regulated and kept at a voltage level to not exceed the maximum input to output voltage differential allowed by the device. The minimum dropout voltage ($V_{IN} – V_O$) must be met with extra headroom when possible to keep the output well regulated. A 0.33-µF or higher capacitor must be placed at the input to bypass noise.

10 Layout

10.1 Layout Guidelines

For the best overall performance, some layout guidelines may be disregarded. Place all circuit components on the same side of the circuit board and as near as practical to the respective linear regulator pins. Traces must be kept short and wide to reduce the amount of parasitic elements in the system. The actual width and thickness of traces depends on the current carrying capability and heat dissipation required by the end system.

10.2 Layout Example

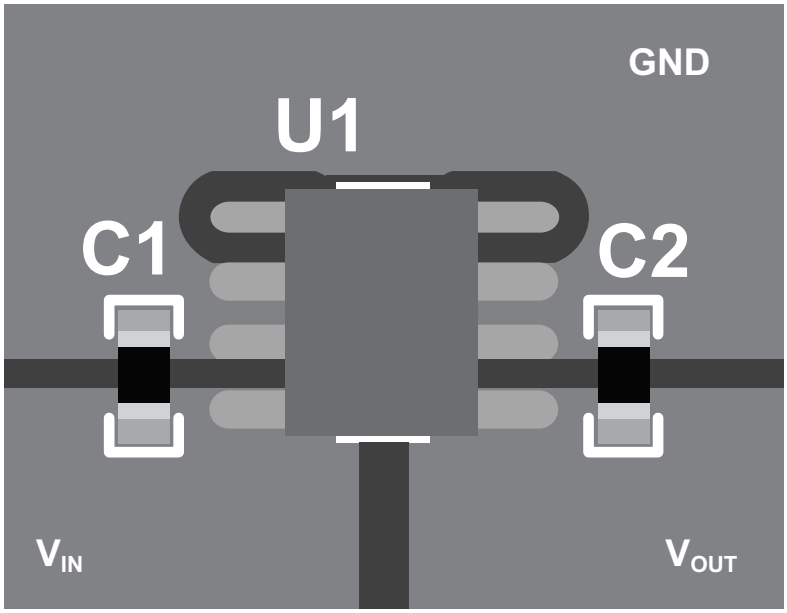


Figure 15. LM78Lxx Example Circuit Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *AN-1112 DSBGA Wafer Level Chip Scale Package* (SNVA009)
- *TO-92 Packing Options / Ordering Instructions* (SNOA072).

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LM78L05	Click here	Click here	Click here	Click here	Click here
LM78L09	Click here	Click here	Click here	Click here	Click here
LM78L12	Click here	Click here	Click here	Click here	Click here
LM78L15	Click here	Click here	Click here	Click here	Click here
LM78L62	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM78L05ACM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 125	LM78L 05ACM	
LM78L05ACM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 125	LM78L 05ACM	Samples
LM78L05ACMX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 125	LM78L 05ACM	
LM78L05ACMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 125	LM78L 05ACM	Samples
LM78L05ACZ/LFT1	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	0 to 125	LM78L 05ACZ	Samples
LM78L05ACZ/LFT3	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	0 to 125	LM78L 05ACZ	Samples
LM78L05ACZ/LFT4	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	0 to 125	LM78L 05ACZ	Samples
LM78L05ACZ/LFT7	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	0 to 125	LM78L 05ACZ	Samples
LM78L05ACZ/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	0 to 125	LM78L 05ACZ	Samples
LM78L05AIM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM78L 05AM	Samples
LM78L05AIMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LM78L 05AM	Samples
LM78L05ITP/NOPB	ACTIVE	DSBGA	YPB	8	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	P 03	Samples
LM78L09ITPX/NOPB	ACTIVE	DSBGA	YPB	8	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	P 02	Samples
LM78L12ACM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 125	LM78L 12ACM	
LM78L12ACM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 125	LM78L 12ACM	Samples
LM78L12ACMX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 125	LM78L 12ACM	
LM78L12ACMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 125	LM78L 12ACM	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM78L12ACZ/LFT3	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	0 to 125	LM78L 12ACZ	Samples
LM78L12ACZ/LFT4	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	0 to 125	LM78L 12ACZ	Samples
LM78L12ACZ/LFT7	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	0 to 125	LM78L 12ACZ	Samples
LM78L12ACZ/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	0 to 125	LM78L 12ACZ	Samples
LM78L15ACM	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 125	LM78L 15ACM	
LM78L15ACM/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 125	LM78L 15ACM	Samples
LM78L15ACMX	NRND	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 125	LM78L 15ACM	
LM78L15ACMX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 125	LM78L 15ACM	Samples
LM78L15ACZ/LFT4	ACTIVE	TO-92	LP	3	2000	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	0 to 125	LM78L 15ACZ	Samples
LM78L15ACZ/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	0 to 125	LM78L 15ACZ	Samples
LM78L62ACZ/NOPB	ACTIVE	TO-92	LP	3	1800	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	0 to 125	LM78L 62ACZ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

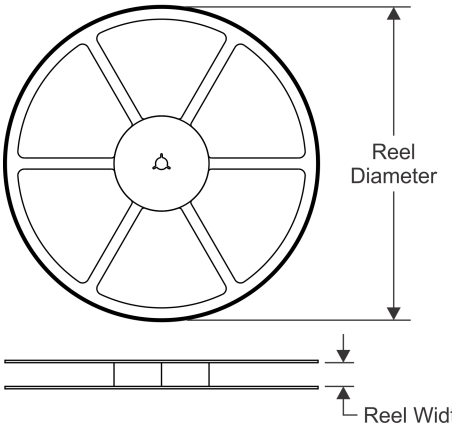
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

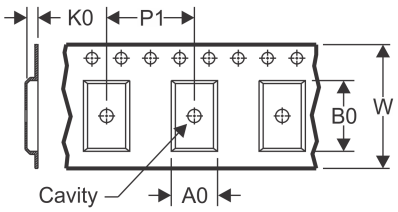
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

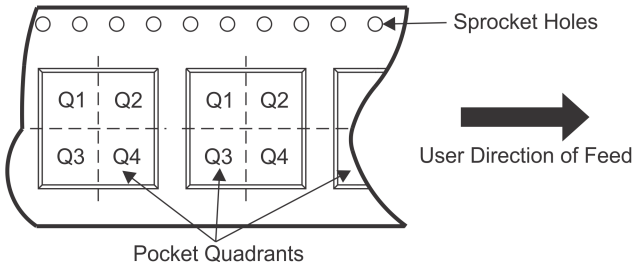


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

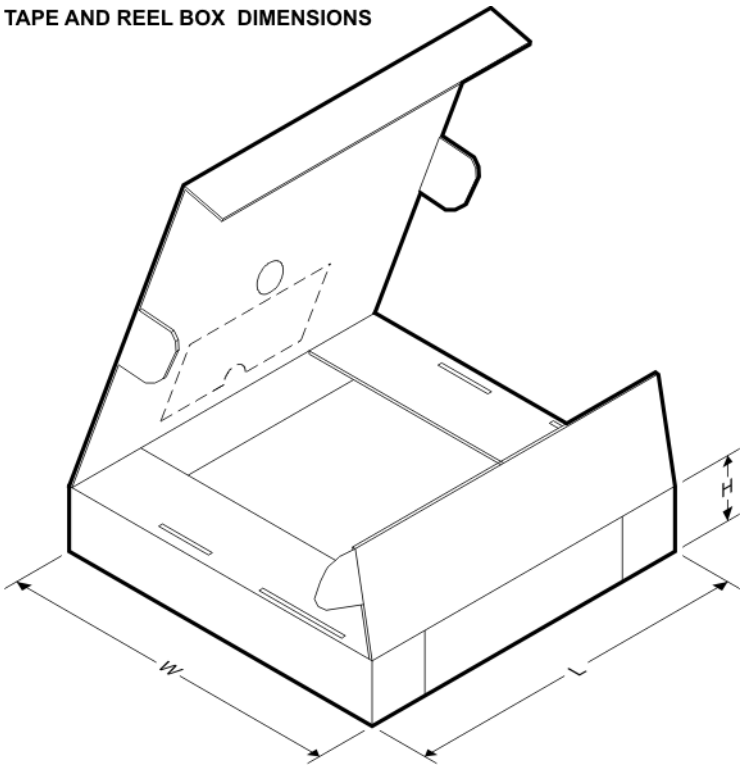
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM78L05ACMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM78L05ACMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM78L05AIMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM78L05ITP/NOPB	DSBGA	YPB	8	250	178.0	8.4	1.5	1.5	0.66	4.0	8.0	Q1
LM78L09ITPX/NOPB	DSBGA	YPB	8	3000	178.0	8.4	1.5	1.5	0.66	4.0	8.0	Q1
LM78L12ACMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM78L12ACMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM78L15ACMX	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LM78L15ACMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

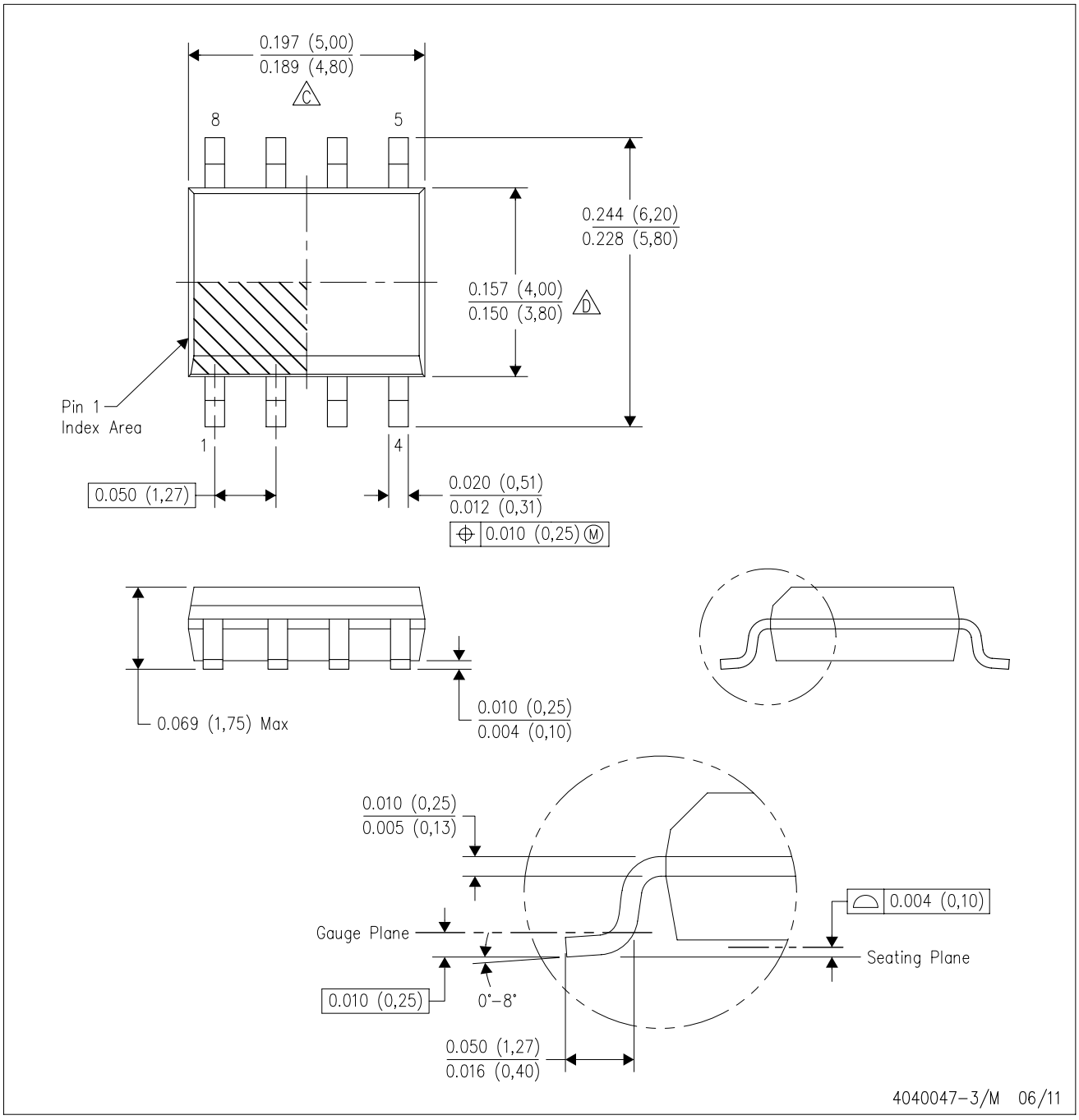
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM78L05ACMX	SOIC	D	8	2500	367.0	367.0	35.0
LM78L05ACMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM78L05AIMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM78L05ITP/NOPB	DSBGA	YPB	8	250	210.0	185.0	35.0
LM78L09ITPX/NOPB	DSBGA	YPB	8	3000	210.0	185.0	35.0
LM78L12ACMX	SOIC	D	8	2500	367.0	367.0	35.0
LM78L12ACMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LM78L15ACMX	SOIC	D	8	2500	367.0	367.0	35.0
LM78L15ACMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

GENERIC PACKAGE VIEW

LP 3 TO-92 - 5.34 mm max height

TRANSISTOR OUTLINE

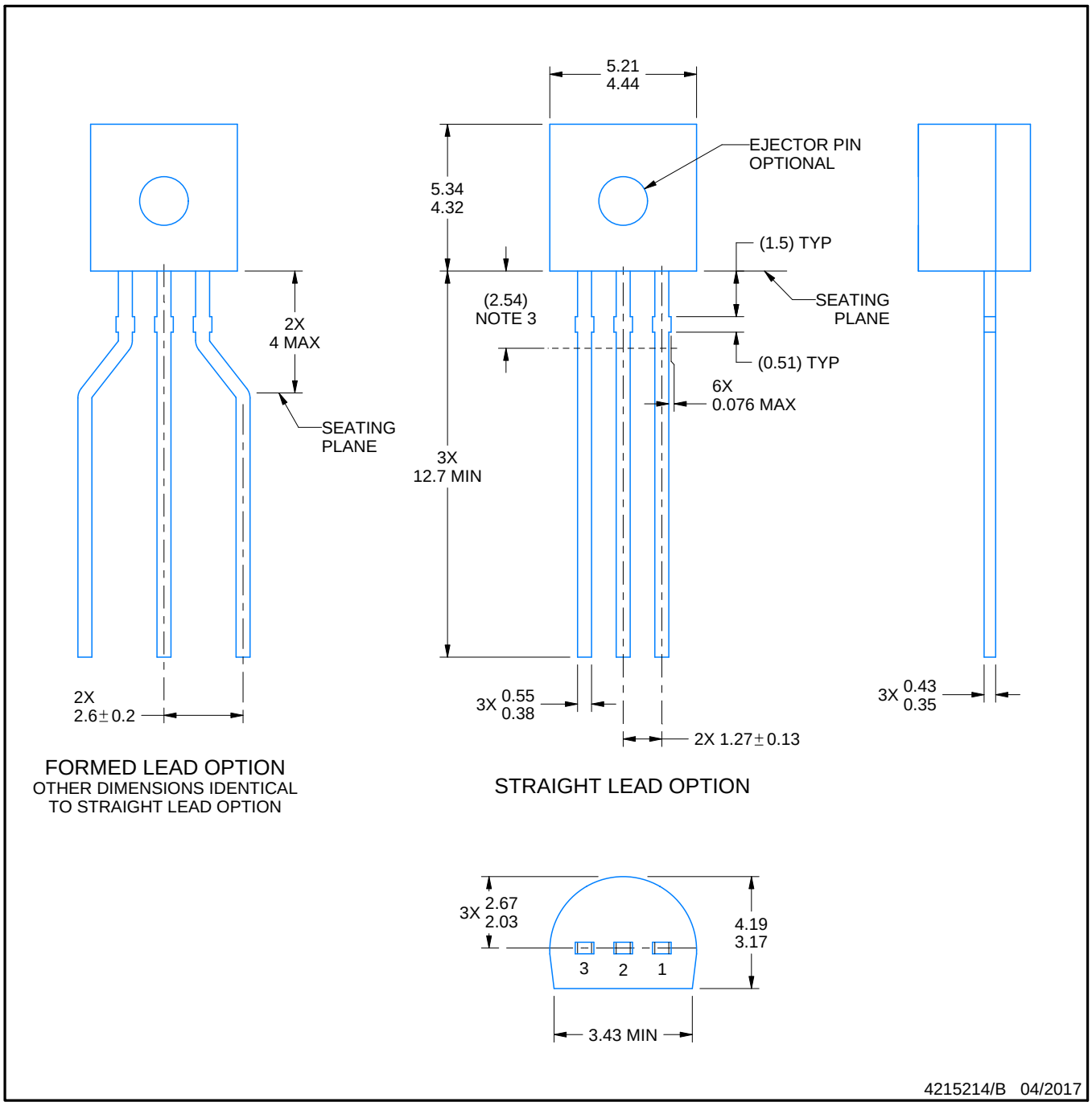
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

LP0003A

PACKAGE OUTLINE

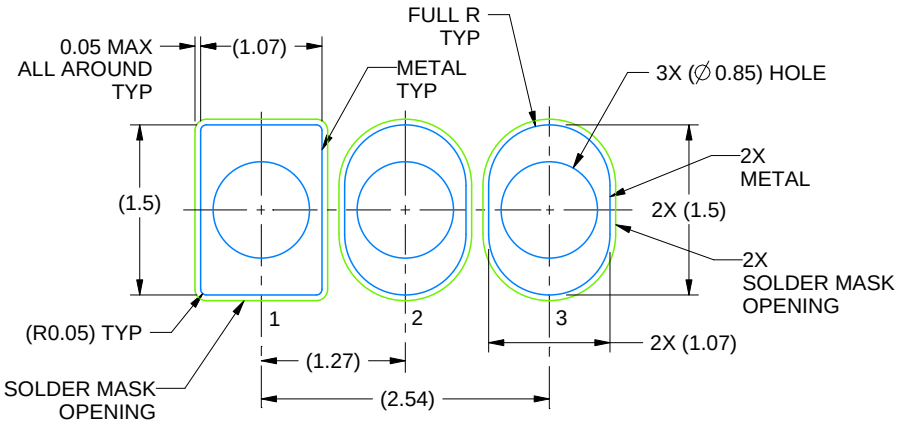
TO-92 - 5.34 mm max height

TO-92

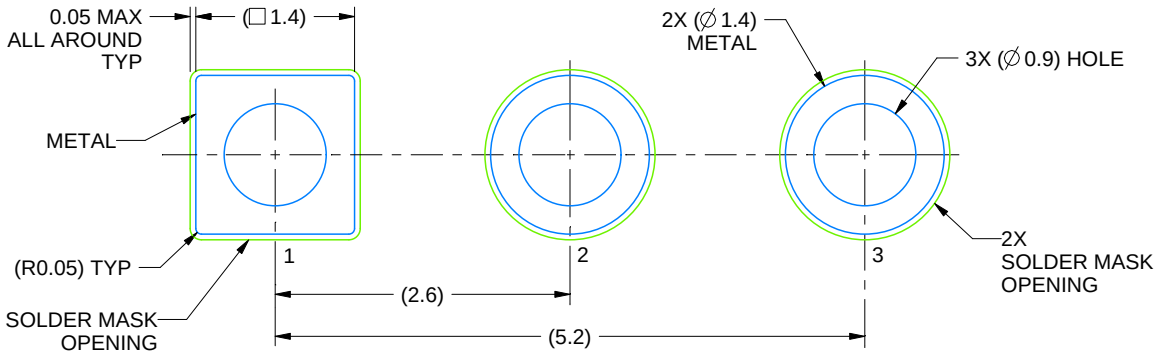


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
   a. Straight lead option available in bulk pack only.
   b. Formed lead option available in tape and reel or ammo pack.
   c. Specific products can be offered in limited combinations of shipping medium and lead options.
   d. Consult product folder for more information on available options.



LAND PATTERN EXAMPLE
STRAIGHT LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X



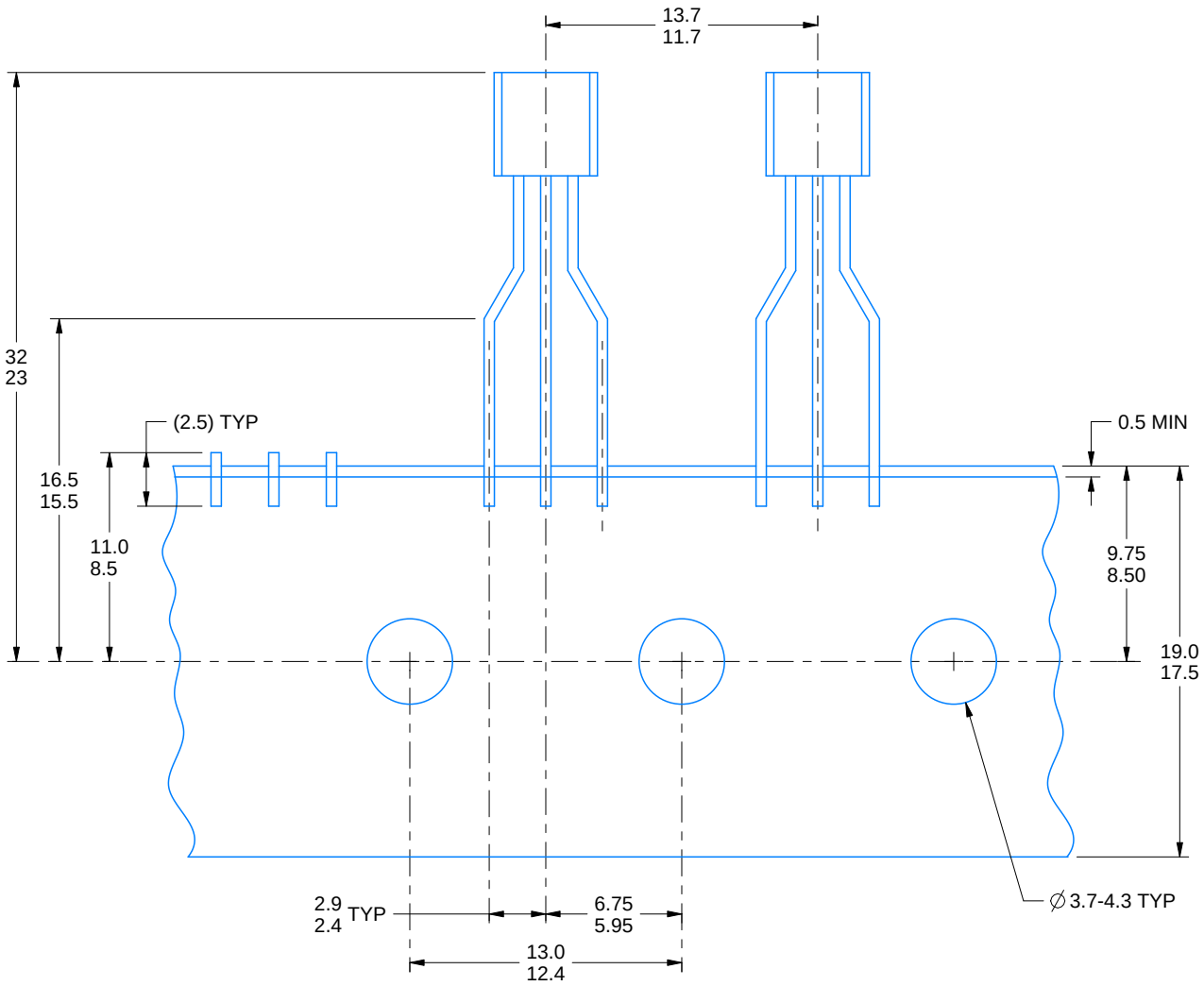
LAND PATTERN EXAMPLE
FORMED LEAD OPTION
NON-SOLDER MASK DEFINED
SCALE:15X

4215214/B 04/2017

LP0003A

TO-92 - 5.34 mm max height

TO-92



FOR FORMED LEAD OPTION PACKAGE

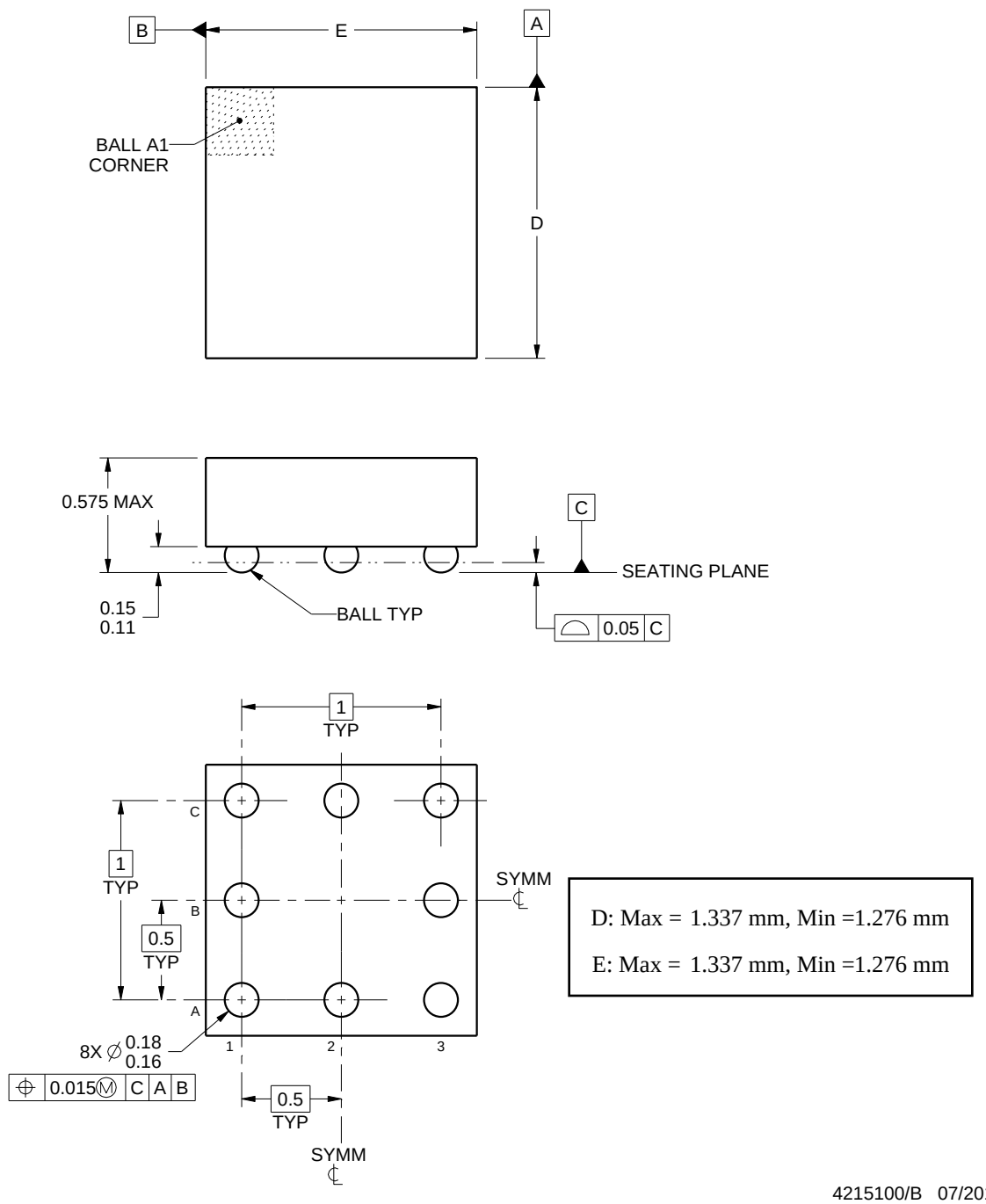
4215214/B 04/2017

PACKAGE OUTLINE

YPB0008

DSBGA - 0.575 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

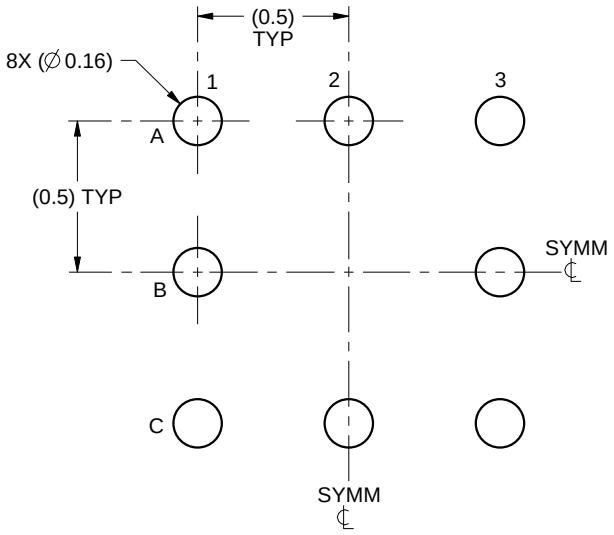
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

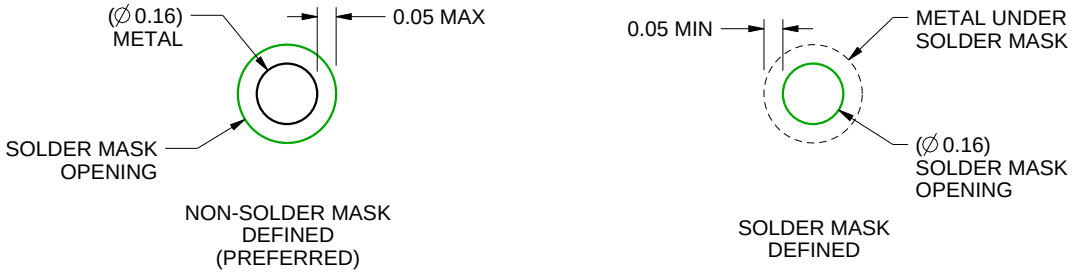
YPB0008

DSBGA - 0.575 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X

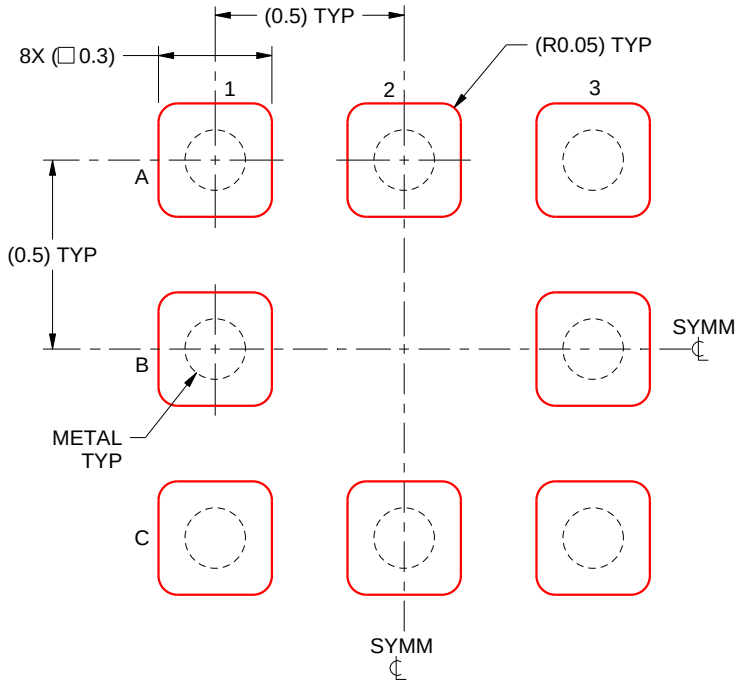


SOLDER MASK DETAILS
NOT TO SCALE

4215100/B 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL
SCALE:50X

4215100/B 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265