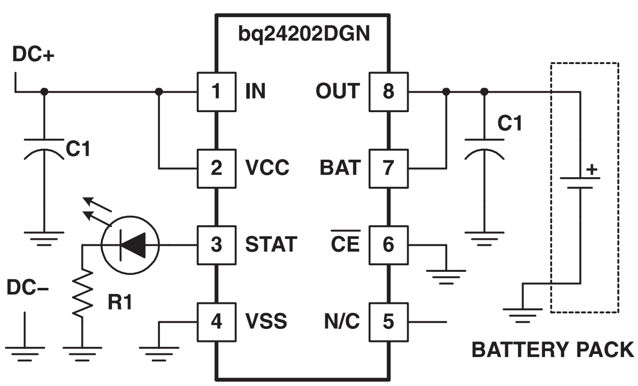
SINGLE-CHIP LI-ION AND LI-POL CHARGE MANAGEMENT IC FOR CURRENT-LIMITED APPLICATIONS

FEATURES

- **Designed Specifically to Work With Current-Limited Wall Supplies**
- **Ideal for Low Dropout Charger Design for Single-Cell Li-Ion Packs With Coke or Graphite Anodes**
- **Integrated PowerFET for 500 mA**
- **Integrated Voltage Regulation With 0.5% Accuracy**
- **Battery Insertion and Removal Detection**
- **Charge Termination by Minimum Current and Time**
- **Pre-Charge Conditioning With Safety Timer**
- **Sleep Mode for Low-Power Consumption**
- **Charge Status Output for LED or Host Processor Interface Indicates**
- **Charge-in-Progress, Charge Completion, and Fault Conditions**
- **Optional Temperature Monitoring Before and During Charge**
- **Small, 8-Pin Power-Pad MSOP Package**

TYPICAL APPLICATION



DESCRIPTION

The bq2420x series are simple Li-Ion linear charge management devices targeted at low-cost and space limited charger applications. The bq2420x series offer integrated powerFET, high-accuracy voltage regulation, temperature monitoring, charge status, and charge termination, in a single monolithic device.

The bq2420x is designed to work with a current-limited wall-mount transformer and therefore does not provide any current regulation. However, these devices offer a fixed internal current limit to prevent damage to the internal powerFET. A time-limited pre-conditioning phase is provided to condition deeply discharged cells. Once the battery reaches the charge voltage, the high accuracy voltage regulation loop takes over and completes the charge cycle. Charge is terminated based on minimum current. An internal charge timer provides a backup safety for charge termination.

Other standard features include an automatic sleep mode activated when V_{CC} falls below the battery voltage and a recharge feature activated when the battery voltage falls below the V_{RCH} threshold.

In addition to the standard features, the core product provides two additional enhancements: temperature monitoring and status display. The temperature-sense circuit continuously measures battery temperature using an external thermistor and inhibits charge until the battery temperature is within the user-defined thresholds. The STAT pin indicates three conditions of operation of the charger. These conditions are *charge-in-progress, charge complete*, and *fault*. This output can be used to drive an LED or an interface to a microcontroller.

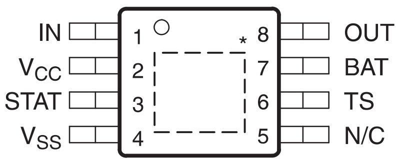
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

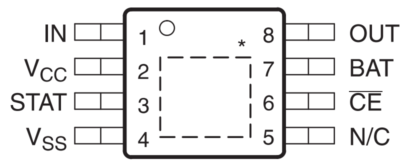
T_J	CHARGE REGULATION VOLTAGE	OPTIONAL FUNCTIONS	MARKING	PACKAGED DEVICES (DGN)(1)
–40°C to 125°C	4.2 V	STAT and TS	AZC	bq24200DGN
	4.1 V	STAT and TS	AZD	bq24201DGN
	4.2 V	STAT	AZE	bq24202DGN
	4.1 V	STAT	AZF	bq24203DGN
	4.2 V	–	AZG	bq24204DGN
	4.1 V	–	AZI	bq24205DGN

(1) The DGN package is available taped and reeled. Add TR suffix to device type (e.g. bq24200DGNTR) to order. Quantities 2500 devices per reel.

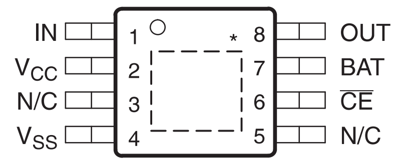
bq24200, bq24201
HTSSOP (DGN) PACKAGE
(TOP VIEW)



bq24202, bq24203
HTSSOP (DGN) PACKAGE
(TOP VIEW)



bq24204, bq24205
HTSSOP (DGN) PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL				I/O	DESCRIPTION
NAME	NO.				
	bq24200 bq24201	bq24202 bq24203	bq24204 bq24205		
BAT	7	7	7	I	Battery voltage sense input
$\overline{CE}$	–	6	6	I	Charge enable input (active low)
IN	1	1	1	I	Charge input voltage
N/C	5	5	3, 5	–	No connection. Must be left floating
OUT	8	8	8	O	Charge current output
STAT	3	3	–	O	Charge status output
TS	6	–	–	I	Temperature sense input
V_{CC}	2	2	2	I	V_{CC} input
V_{SS}	4	4	4	–	Ground input

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
	Supply voltage (Vcc with respect to GND)	16.5	V
	Input voltage, IN, STAT, TS (all with respect to GND)	16.5	V
	Input voltage, BAT, OUT (all with respect to GND)	7	V
	Output sink/source current (STAT)	15	mA
T_{stg}	Storage temperature range	–65 to 150	°C
T_J	Junction temperature range	–40 to 125	°C
	Lead temperature (soldering, 10 sec)	300	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT (θ_{JA})	THERMAL IMPEDANCE JUNCTION-TO-CASE (θ_{JC})	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$
8 Pin DGN[1]	57.20°C/W	4.4°C/W	1.75 W	0.017 W/°C

(1) This data is based on using JEDEC High-K board and topside traces, top and bottom thermal pad (2 mm × 3 mm), internal 1 oz. power and ground planes, four thermal via underneath the die connecting to ground plane.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{CC}	Supply voltage	$V_{(LOWV-MIN)}$	13.5	V
V_{IN}	Input voltage	$V_{(LOWV-MIN)}$	13.5	V
T_J	Operating junction temperature range	–40	125	°C

ELECTRICAL CHARACTERISTICS

over 0°C ≤ T_J ≤ 125°C and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC(VCC)}$	Vcc Current	Vcc > Vcc(min)		1.7	2.5	mA
$I_{CC(SLP)}$	Sleep current	Sum of currents into OUT and BAT pins, Vcc < $V_{(SLP)}$, 0°C ≤ T_J ≤ 85°C			5	µA
		Sum of currents into OUT and BAT pins, Vcc < $V_{(SLP)}$			10	µA
$I_{CC(STDBY)}$	Standby current	Sum of currents into Vcc, IN and TS pins, (Vcc–$V_{I(TS)}$) ≤ 300 mV			1	mA
$I_{IB(BAT)}$	Input bias current on BAT pin				1	µA
$I_{IB(TB)}$	Input bias current on TS pin	0.1 × Vcc ≤ $V_{I(TS)}$ ≤ 0.8 × Vcc			1	µA

VOLTAGE REGULATION

$V_{O(REG)} + V_{(DO.MAX)} \leq VCC$, $I_{(TERM)} < I_{O(OUT)} \leq 500$ mA, over 0°C ≤ T_J ≤125°C and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{O(REG)}$	Output voltage	$V_{O(REG)} + V_{(DO–MAX)} \leq 10$ V, $I_{(TERM)} < I_{O(OUT)} \leq 250$ mA	4.0795	4.10	4.1205	V
			4.05	4.10	4.15	V
		$V_{O(REG)} + V_{(DO–MAX)} \leq 10$ V, $I_{(TERM)} < I_{O(OUT)} \leq 250$ mA	4.1790	4.20	4.2210	V
			4.15	4.20	4.25	V
$V_{(DO)}$	Dropout voltage ($V_{(IN)} – V_{(OUT)}$)	$V_{O(REG)} + V_{(DO–MAX)} \leq$ Vcc, $I_{O(OUT)}$ = 500 mA	200	350	500	mV

TEXAS INSTRUMENTS
www.ti.com

OUTPUT CURRENT

over 0°C ≤ T_J ≤ 125°C and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{O(OUT)}$	Output current	See (1)			500	mA
$I_{(SC)}$	Short-circuit trip current	See (1)	1		1.6	A

(1) Assured by design, not production tested.

PRE-CHARGE CURRENT REGULATION

over 0°C ≤ T_J ≤ 125°C and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(PRECHG)}$	Pre-charge current	$V_{I(BAT)} < V_{(LOWV)}$, $t < t_{(30min)}$	10	13.5	19	mA
$I_{(DETECT)}$	Battery detection current	$V_{I(BAT)}$ < 2.5 V, $t < t_{(30min)}$	160	210	300	µA

CHARGE TERMINATION DETECTION

over 0°C ≤ T_J ≤ 125°C and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(TAPER)}$	Taper current detect threshold	$V_{I(BAT)} > V_{(RCH)}$	21	25.5	31	mA
$I_{(TERM)}$	Charge termination current detect threshold	$V_{I(BAT)} > V_{(RCH)}$	0.8	1.1	1.4	mA

TEMPERATURE COMPARATOR

over 0°C ≤ T_J ≤ 125°C and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(TS1)}$	Lower temperature threshold	TS pin voltage		30		%VCC
$V_{(TS2)}$	Upper temperature threshold	TS pin voltage		60		%VCC
	Accuracy		–0.7		0.7	%VCC
	Hysteresis			1		%VCC

LOW VOLTAGE BATTERY THRESHOLD

over 0°C ≤ T_J ≤ 125°C and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(LOWV)}$	LowV threshold	0°C ≤ T_J ≤ 85°C	2.8	2.95	3.1	V
			2.8	3.0	3.2	V

BATTERY RECHARGE THRESHOLD

over 0°C ≤ T_J ≤ 125°C and supply voltage range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Recharge threshold, V_{RCH} (typically 100 mV below regulation)		$V_{O(REG)}$ –0.115	$V_{O(REG)}$ –0.1	$V_{O(REG)}$ –0.085	V

STAT OUTPUT

Vcc ≥ $V_{O(REG)}$, over 0°C ≤ T_J ≤ 125°C and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OL(STAT)}$	Output (low) saturation voltage	I_O = 10 mA			0.5	V
$V_{OH(STAT)}$	Output (high) saturation voltage	I_O = –5 mA	Vcc–1.5			V

$\overline{CE}$

over 0°C ≤ T_J ≤ 125°C and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IL(CE)}$	Input (low) voltage	I_{IL} = 5 µA	0		Vcc–1	V
$V_{IH(CE)}$	Input (high) voltage	I_{IH} = 20 µA	Vcc–0.3			V

TIMERS

over 0°C ≤ T_J ≤ 125°C and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(PRECHG)}$	Pre-charge and taper timer		1,548	2,065	2,581	sec
$t_{(TAPER)}$	Taper timer		1,548	2,065	2,581	sec
$t_{(CHG)}$	Charge timer		9,292	12,389	15,486	sec

SLEEP COMPARATOR

over 0°C ≤ T_J ≤ 125°C and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SLP)}$	Sleep-mode threshold	2.3 V ≤ $V_{I(BAT)}$ ≤ $V_{O(REG)}$	V(BAT) –10mV			V

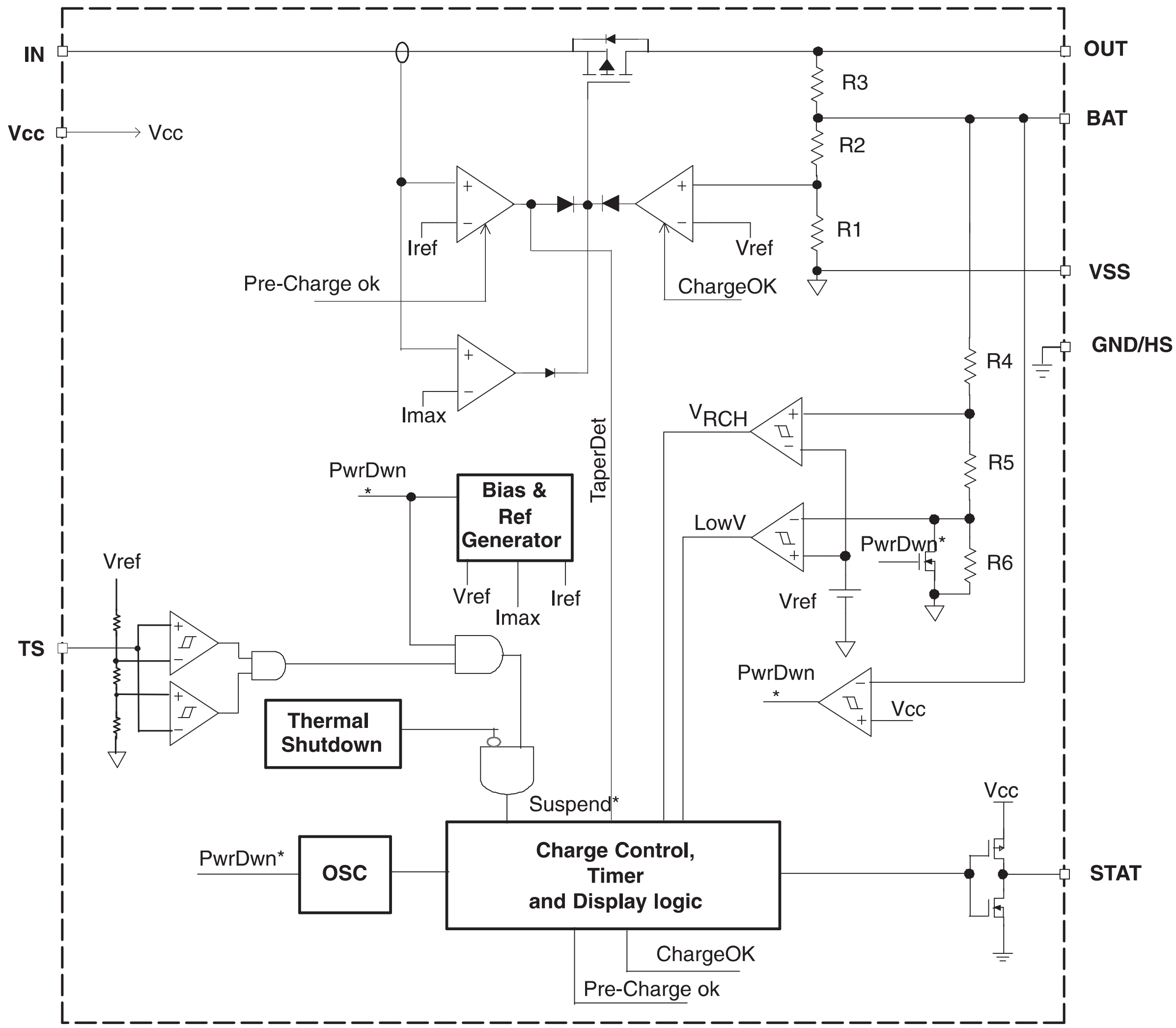
POWER-ON-RESET AND V_{IN} RAMP RATE

over 0°C ≤ T_J ≤ 125°C and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{POR}	POR threshold	See [(1)]	2.3	2.4	2.5	V
	Slew rate	See [(1)]	5		5×10^{-5}	V/µs

(1) Ensured by design, not production tested.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

IN: This pin is connected to the source of the internal P-channel powerFET.

OUT: This pin is connected to the drain of the internal P-channel powerFET.

Battery voltage sense (BAT): Voltage sense-input tied directly to the positive side of the battery.

Temperature sense input (TS): Input for an external battery-temperature monitoring circuit.

Charge status output (STAT): High-impedance indication of various charge conditions.

Supply voltage input (VCC): Power supply input

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
JUNCTION TEMPERATURE

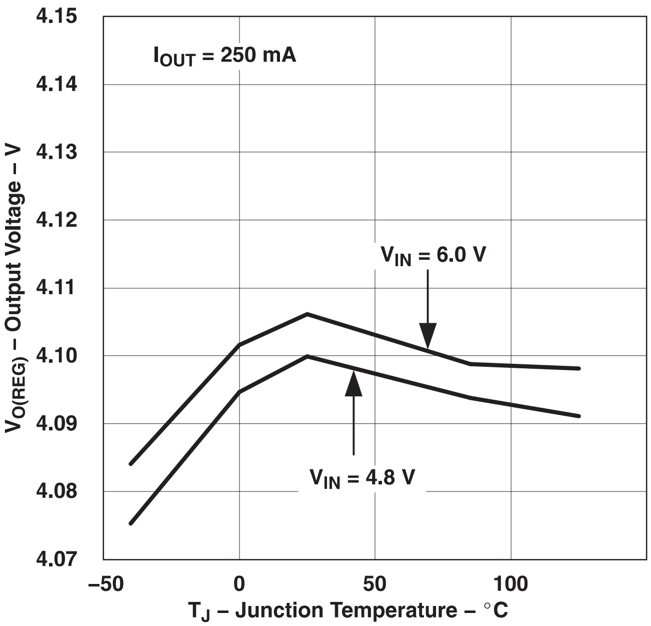


Figure 1.

DROPOUT VOLTAGE
vs
JUNCTION TEMPERATURE

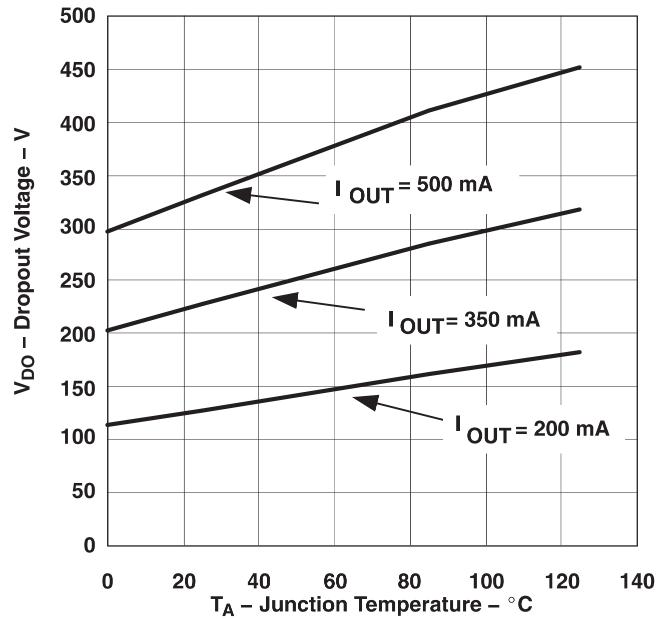


Figure 2.

DROPOUT VOLTAGE
vs
OUTPUT VOLTAGE

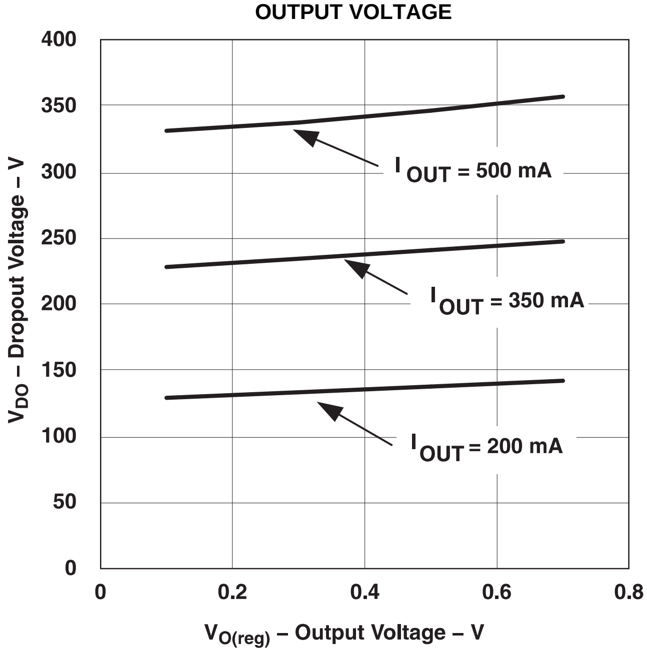


Figure 3.

SUPPLY CURRENT
vs
JUNCTION TEMPERATURE

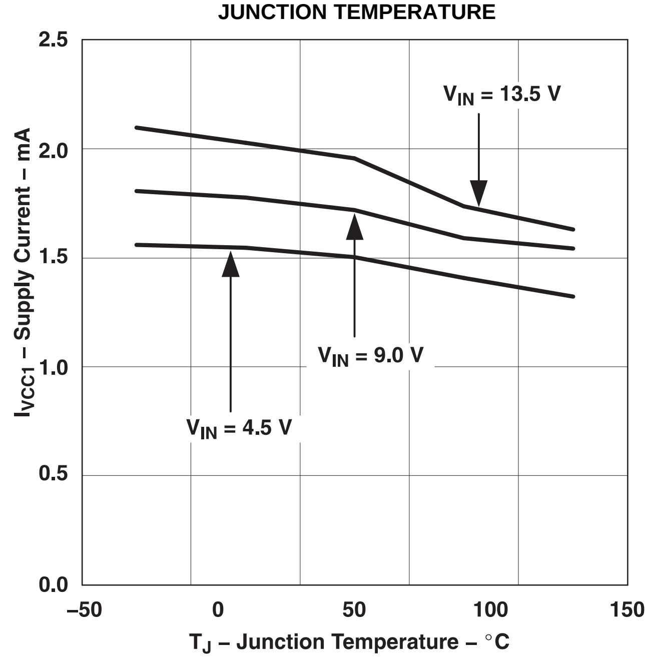


Figure 4.

APPLICATION INFORMATION

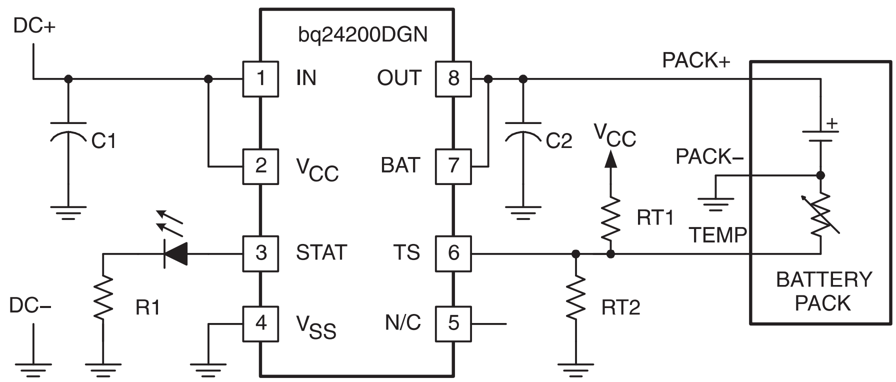


Figure 5. Low Dropout Single-Cell Li-Ion/Li-Pol Charger

FUNCTIONAL DESCRIPTION

The bq2420x supports a precision Li-Ion or Li-Pol charging system suitable for single-cells with either coke or graphite anodes. Figure 5 shows an application schematic and Figure 6 shows the typical charge profile.

TEMPERATURE QUALIFICATION (bq24200 and bq24202 only)

The bq24200 and bq24201 continuously monitors battery temperature by measuring the voltage between the TS and VSS pins. A negative- or a positive-temperature coefficient thermistor (NTC, PTC) and an external voltage divider typically develop this voltage (see Figure 5). The bq24200 and bq24201 compare this voltage against the internal $V_{(TS1)}$ and $V_{(TS2)}$ thresholds to determine if charging is allowed (see Figure 7). The temperature sensing circuit is immune to any fluctuation in Vcc since both the external voltage divider and the internal thresholds are referenced to Vcc.

Once a temperature outside the $V_{(TS1)}$ and $V_{(TS2)}$ thresholds is detected the bq24200 and bq24201 immediately suspend the charge. The bq24200 and bq24201 suspend the charge by turning off the power FET and holding the timer value (i.e., timers are NOT reset). Charge is resumed when the temperature returns to the normal range.

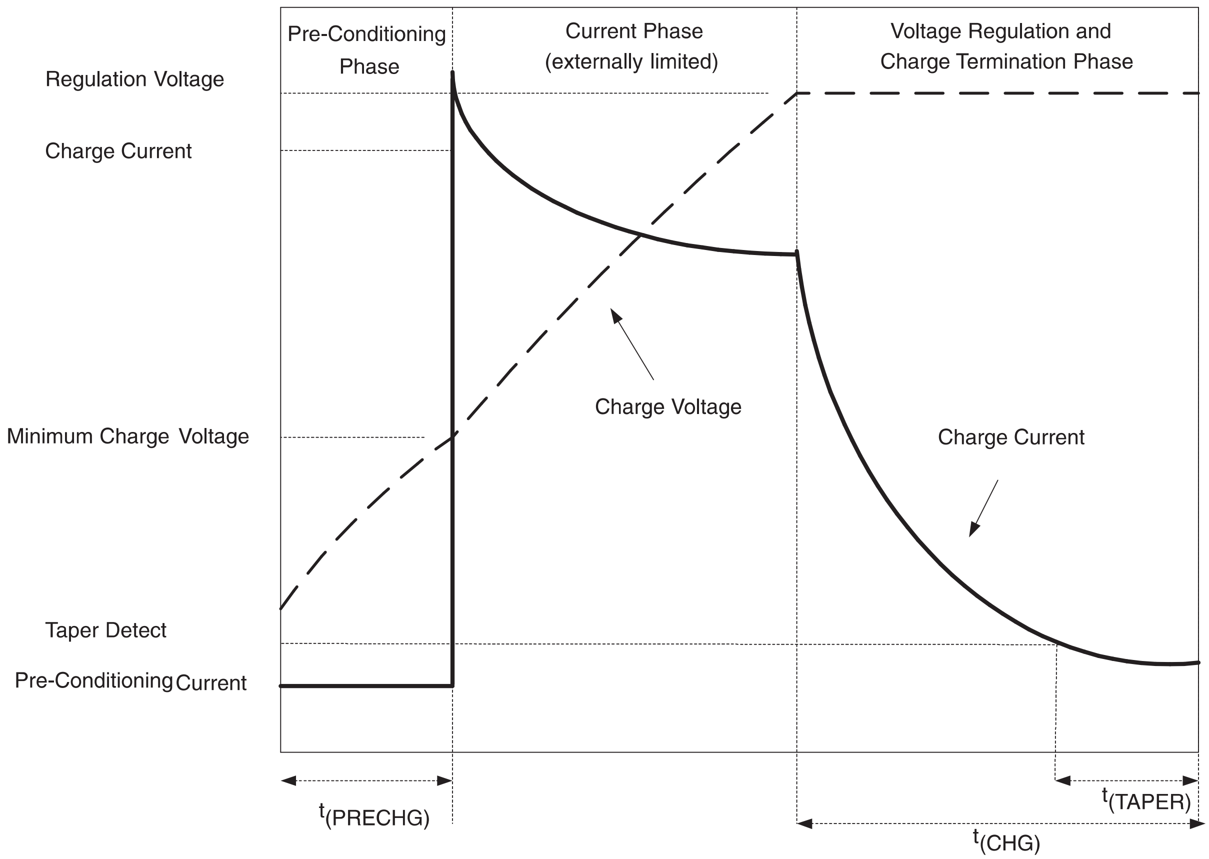


Figure 6. Typical Charge Profile

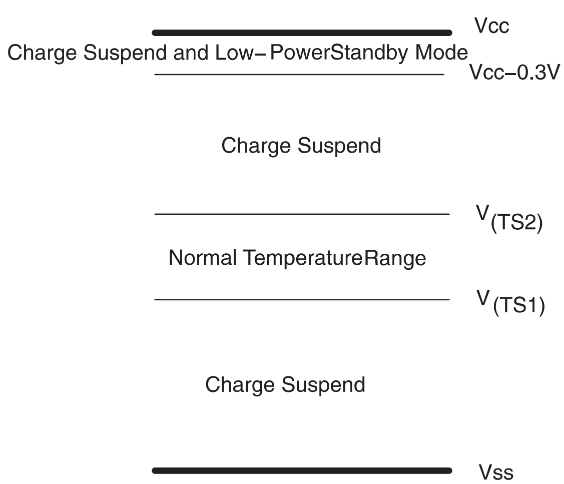


Figure 7. TS Pin Thresholds

OPERATIONAL FLOW DIAGRAM

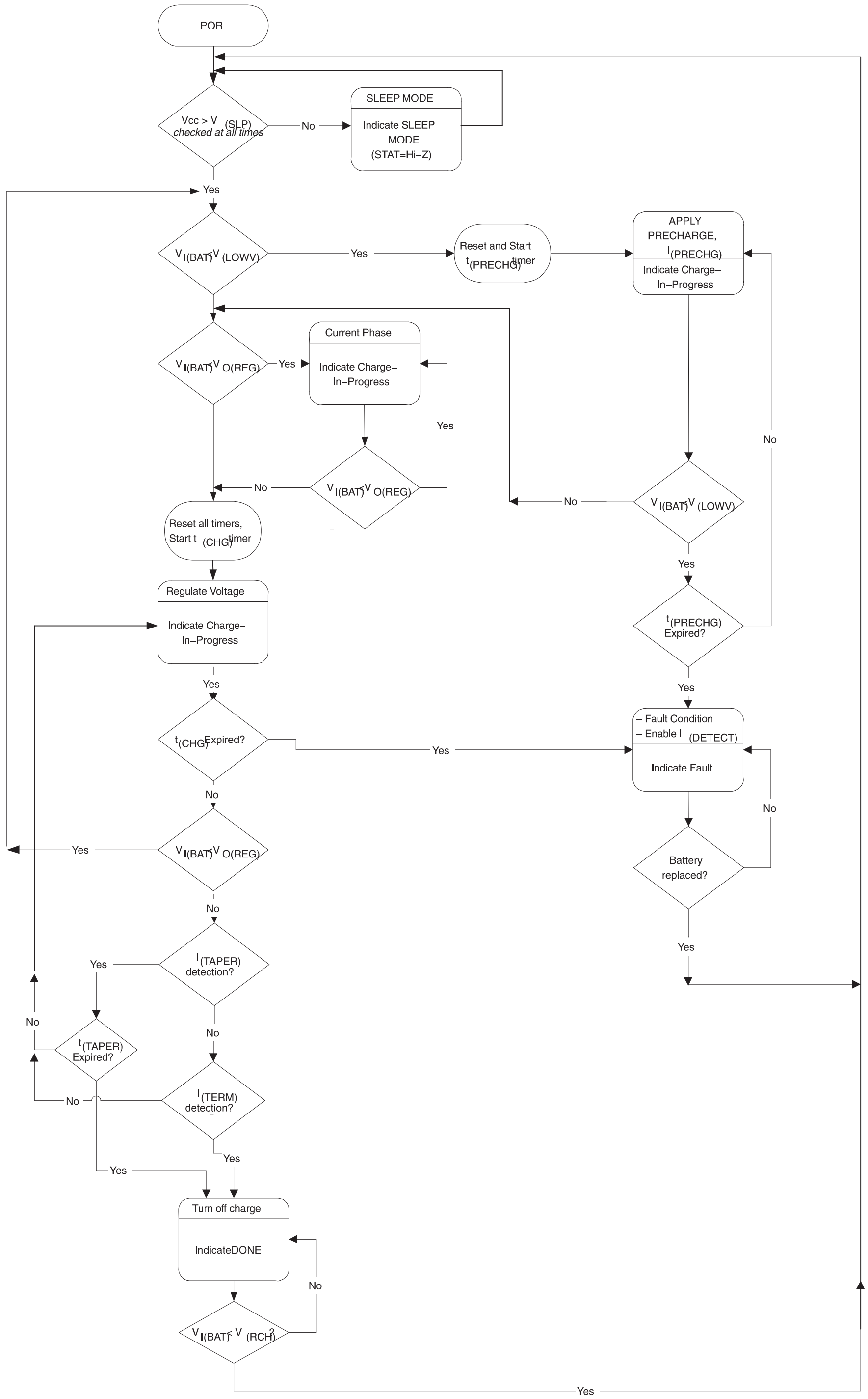


Figure 8. Operational Flow Chart

The resistor values of RT1 and RT2 are calculated by the following equations:

For NTC Thermistors:

$$R_{T1} = \frac{\left(5 \times RT_H \times RT_C\right)}{\left(3 \times \left(RT_C - RT_H\right)\right)} \tag{1}$$

$$R_{T2} = \frac{\left(5 \times RT_H \times RT_C\right)}{\left(2 \times RT_C\right) - \left(7 \times RT_H\right)} \tag{2}$$

For PTC Thermisters:

$$R_{T1} = \frac{\left(5 \times RT_H \times RT_C\right)}{\left(3 \times \left(RT_H - RT_C\right)\right)} \tag{3}$$

$$R_{T2} = \frac{\left(5 \times RT_H \times RT_C\right)}{\left(2 \times RT_H\right) - \left(7 \times RT_C\right)} \tag{4}$$

Where RT_C is the cold temperature resistance and RT_H is the hot temperature resistance of thermistor, as specified by the thermistor manufacturer.

R_{T1} or R_{T2} can be omitted If only one temperature (hot or cold) setting is required. Applying a voltage between the V_{TS1} and V_{TS2} thresholds to pin TS disables the temperature-sensing feature. Also applying a voltage between (V_{CC} – 0.3 V) and Vcc suspends the charge and places the IC in the low-power standby mode.

BATTERY PRE-CONDITIONING

Figure 7 shows the operational flow chart for the bq2420x.

Upon power-up, if the battery voltage is below the $V_{(LOWV)}$ threshold, the bq2420x applies a pre-charge current, $I_{(PRECHG)}$, to the battery. This feature revives deeply discharged cells. The bq2420x activates a safety timer, $t_{(PRECHG)}$, during the conditioning phase. If $V_{(LOWV)}$ threshold is not reached within the timer period, the bq2420x turns off the charger and enunciates FAULT on the STAT pin. In the case of a FAULT condition, the bq2420x reduces the current to $I_{(DETECT)}$. $I_{(DETECT)}$ is used to detect a battery replacement condition. Fault condition is cleared by POR or battery replacement.

BATTERY CHARGE CURRENT

Following a successful pre-conditioning, the bq2420x relies on an external current-limited supply to limit the charge current to the cell. The bq2420x continues this phase until the battery reaches the voltage regulation phase.

During this phase (and all other phases of operation) in order to protect the integrated powerFET, the internal short circuit and thermal protection circuits are active.

BATTERY VOLTAGE REGULATION

The voltage regulation feedback is through the BAT pin. This input is tied directly to the positive side of the battery pack. The bq2420x monitors the battery-pack voltage between the BAT and VSS pins. The bq2420x is offered in two fixed-voltage versions: 4.1 V and 4.2 V.

As a safety backup, the bq2420x also monitors the charge time in the voltage regulation mode. If taper current is not detected within this time period, $t_{(CHG)}$, the bq2420x turns off the charger and enunciates FAULT on the STAT pin. Fault condition is cleared by POR or battery replacement. Note that the safety timer is reset if the bq2420x is forced out of the voltage regulation mode.

CHARGE TERMINATION AND RECHARGE

The bq2420x monitors the charging current during the voltage regulation phase. Once the taper threshold, $I_{(TAPER)}$, is detected the bq2420x initiates the taper timer, $t_{(TAPER)}$. Charge is terminated after the timer expires. The bq2420x resets the taper timer in the event that the charge current returns above the taper threshold, $I_{(TAPER)}$.

In addition to the taper current detection, the bq2420x terminates charge in the event that the charge current falls below the $I_{(TERM)}$ threshold. This feature allows for quick recognition of a battery removal condition.

After a charge termination, the bq2420x restarts the charge once the voltage on the BAT pin falls below the $V_{(RCH)}$ threshold. This feature keeps the battery at full capacity at all times.

SLEEP MODE

The bq2420x enters the low-power sleep mode if the Vcc is removed from the circuit (i.e., the Vcc and IN pins are floating). For applications where these pins are not floating, placing a low-power 10 Ω (1/16 W) between the IN and VCC pins ensures the $V_{(SLP)}$ conditions are met (see Figure 9).This feature prevents draining the battery during the absence of V_{CC}.

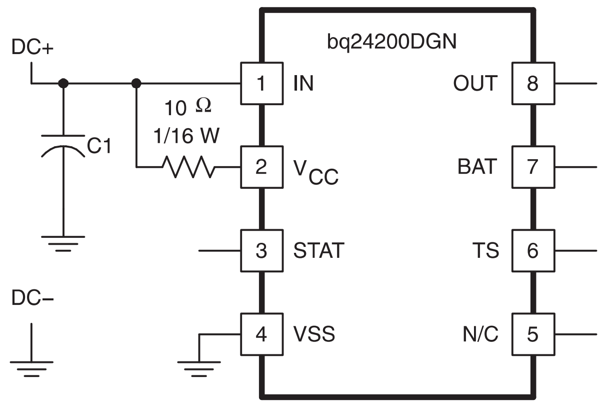


Figure 9. Sleep Mode

CHARGE ENABLE PIN

The $\overline{CE}$ pin on bq24202, bq24203, bq24204 and bq24205 can be used to enable or suspend the charge. Charge is enabled if the voltage $V_{IL(CE)}$ is applied to the pin. Applying the $V_{IH(CE)}$ suspends the charge. During a charge suspend mode, the internal powerFET is turned off and all timers are reset.

CHARGE STATUS OUTPUT

The STAT pin on the bq2420x, indicates various conditions of operation. These conditions are summarized in Table 1.

Table 1. STAT Pin

CONDITION	STAT
Pre-charge	High
Fast-charge	High
Charge-complete	Low
Taper timer done	Low
Charge suspend (due to temperature or $\overline{CE}$ input)	Hi-Z
Thermal shutdown	Hi-Z
Pre-charge timer fault	Hi-Z
Sleep mode	Hi-Z
Charge timer fault	Hi-Z

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24200DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZC	Samples
BQ24200DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZC	Samples
BQ24200DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZC	Samples
BQ24201DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZD	Samples
BQ24202DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZE	Samples
BQ24202DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZE	Samples
BQ24202DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZE	Samples
BQ24202DGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZE	Samples
BQ24203DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZF	Samples
BQ24203DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZF	Samples
BQ24204DGN	LIFEBUY	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZG	
BQ24205DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AZI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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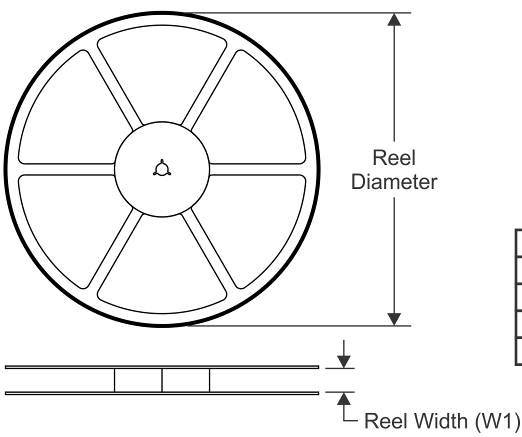
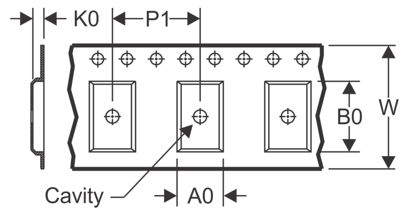
TAPE AND REEL INFORMATION

REEL DIMENSIONS

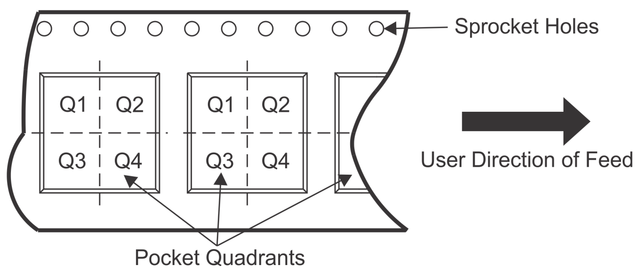


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

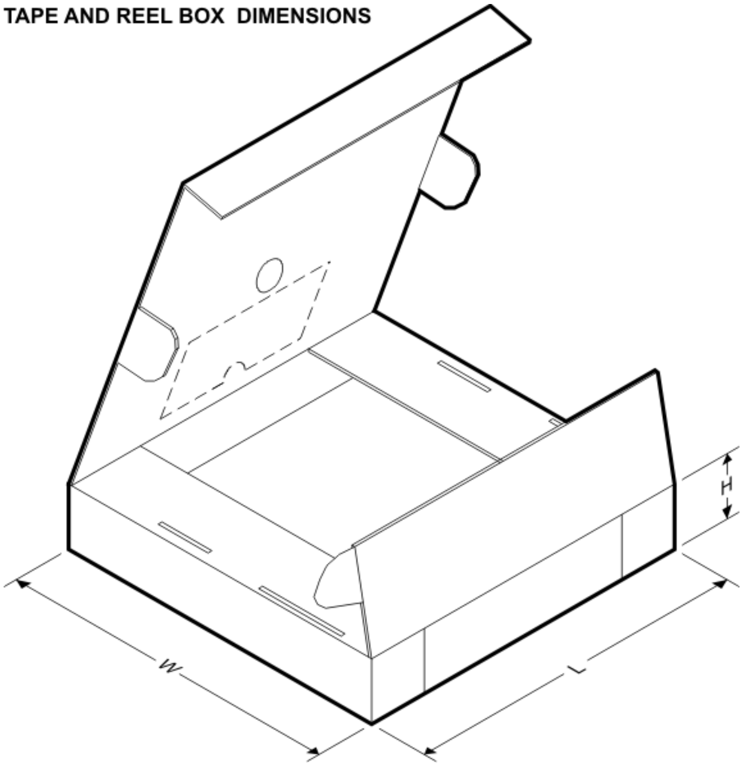
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24200DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
BQ24202DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

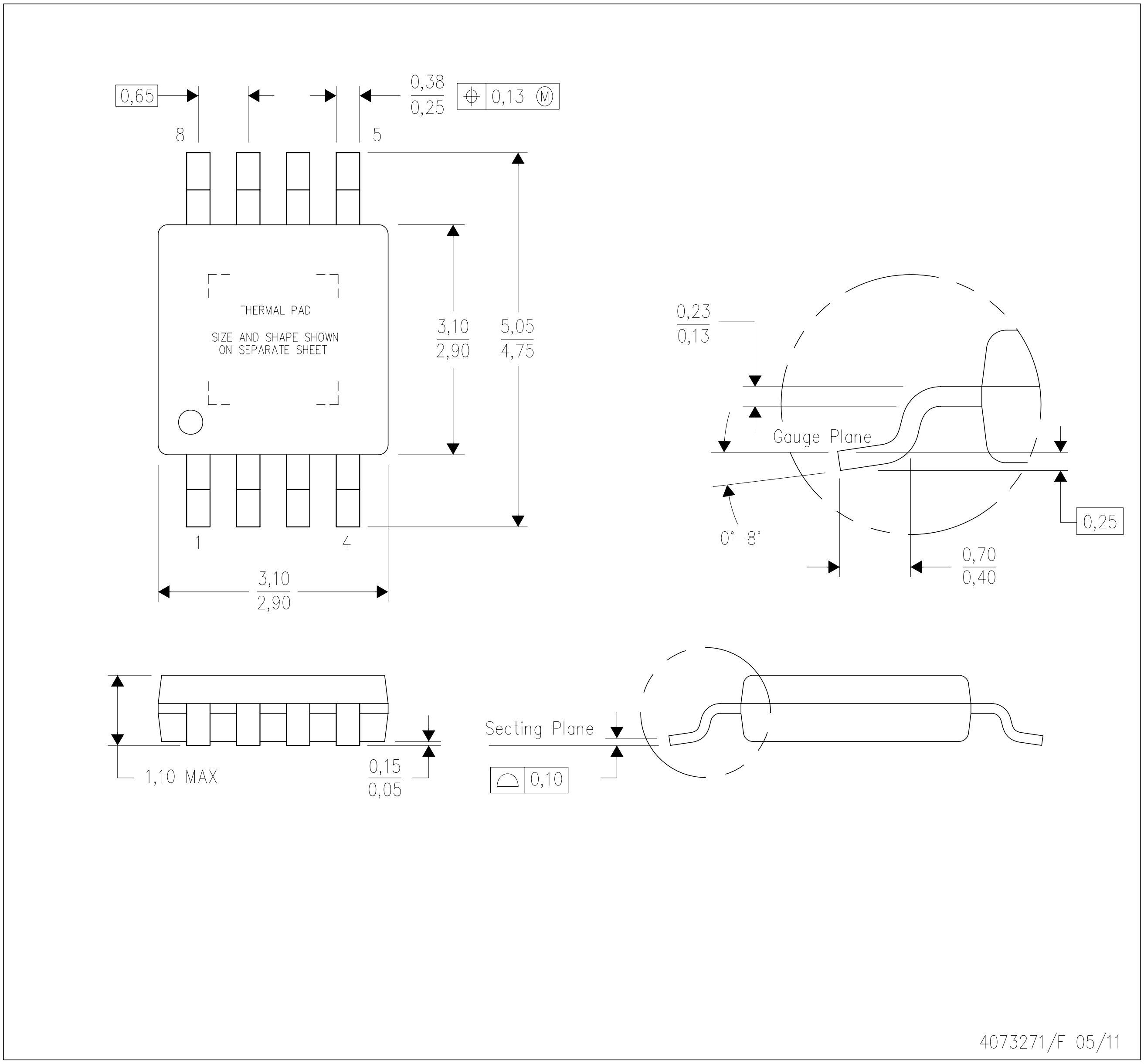
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24200DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
BQ24202DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0

DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO–187 variation AA–T

PowerPAD is a trademark of Texas Instruments.

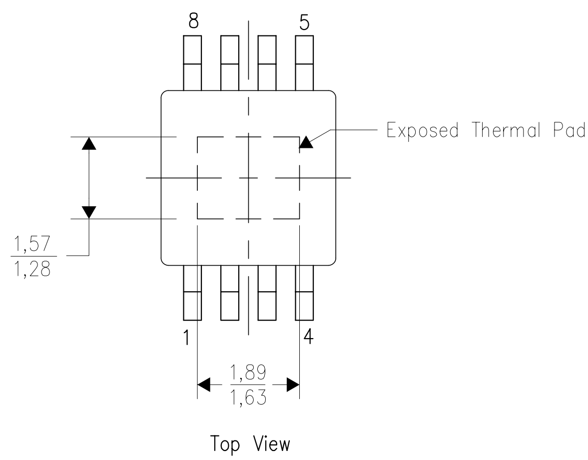
DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



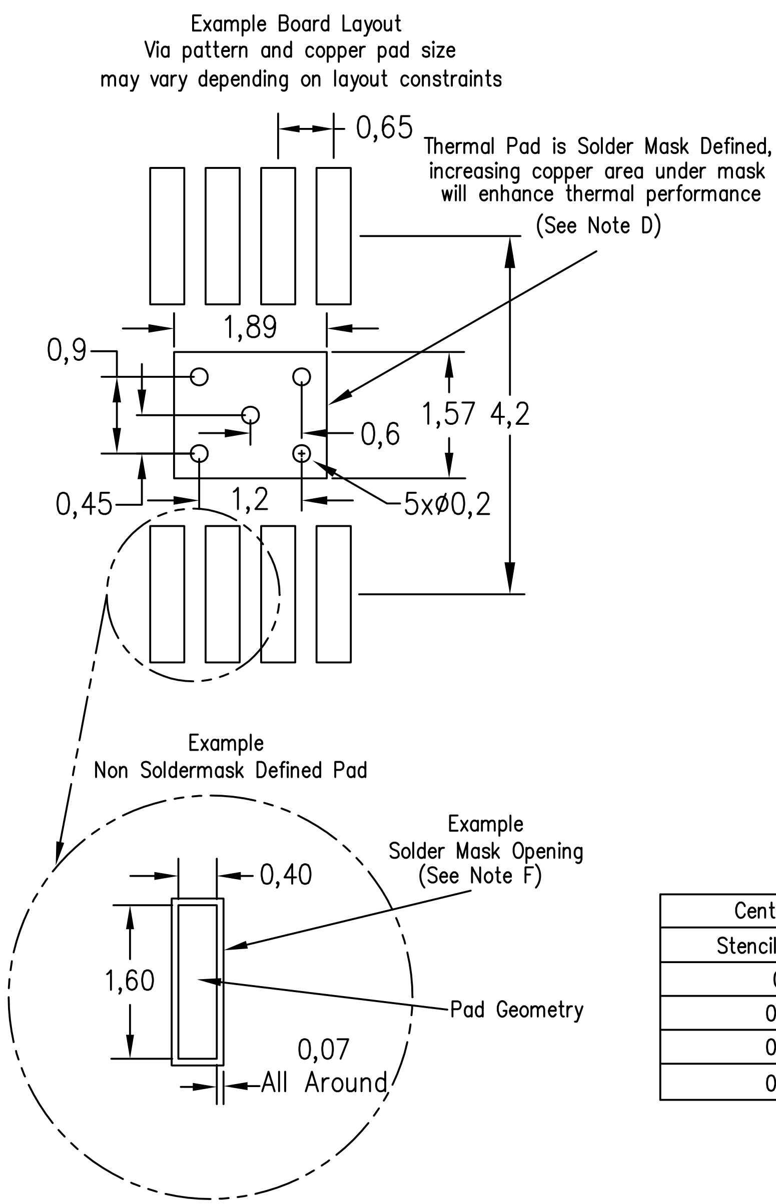
Exposed Thermal Pad Dimensions

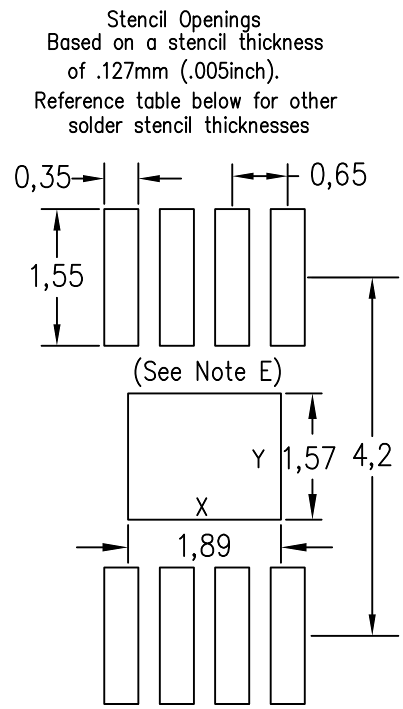
4206323-2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE





Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737-2/F 02/13

NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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