Feature	MitySOM-5CSX	MitySOM-335x	MityDSP-L138(F)[7] LX16	MityDSP-L138(F)[7] LX45	MitySOM-1808(F)/ 1810(F)[7] LX16	MityDSP-6748F LX16	MityDSP-6455F 4000	MityDSP-6455F 2000	MityDSP-6711F-XM	MityDSP-6711F
TI DSP Processor	**None**	**None**	**C674x**	**C674x**	**None**	**C674x**	**C6454 / 55[5]**	**C6454 / 55[5]**	**C6711**	**C6711**
Max Speed	---	---	456 MHz	456 MHz	---	456 MHz	1200 MHz	1200 MHz	200 MHz	200 MHz
L1 Program Cache	---	---	32 KB	32 KB	---	32 KB	32 KB	32 KB	4 KB	4 KB
L1 Data Cache	---	---	32 KB	32 KB	---	32 KB	32 KB	32 KB	4 KB	4 KB
Internal RAM	---	---	256 KB	256 KB	---	256 KB	2048 KB	2048 KB	64 KB	64 KB
ARM Processor	**Cortex-A9**	**Cortex-A8**	**ARM926EJ-S**	**ARM926EJ-S**	**ARM926EJ-S**	**None**	**None**	**None**	**None**	**None**
Cores	**Dual**	**Single**	**Single**	**Single**	**Single**	**---**	**---**	**---**	**---**	**---**
Max Speed	925 MHz	1000 MHz	456 MHz	456 MHz	456 MHz	---	---	---	---	---
L1 Program Cache	32 KB (per core)	32 KB	16 KB	16 KB	16 KB	---	---	---	---	---
L1 Data Cache	32 KB (per core)	32 KB	16 KB	16 KB	16 KB	---	---	---	---	---
L2 Cache	512 KB (shared)	256 KB	256 KB	256 KB	256 KB	---	---	---	---	---
Internal RAM	64 KB	64 KB	8 KB	8 KB	8 KB	---	---	---	---	---
FPGA	**5CSXC6**	**None**	**XC6SLX16[4]**	**XC6SLX45[4]**	**XC6SLX16[4]**	**XC6SLX16[4]**	**X3CS4000**	**X3CS2000**	**XC3S1000**	**XC3S400**
Slices	110,000 LE	---	2,278	6,822	2,278	2,278	27,648	20,480	7,680	3,584
Logic Cells	41,509 ALM	---	14,579	43,661	14,579	14,579	62,208	46,080	17,280	8,064
Block RAM	621 Kb MLABs	---	576 Kb	2,088 Kb	576 Kb	576 Kb	1,728 Kb	720 Kb	432 Kb	288 Kb
Memory										
Max CPU RAM	4 GB	1 GB	256 MB	256 MB	256 MB	128 MB	128 MB	128 MB	32 MB	8 MB
CPU RAM Throughput	TBD	800 MB/sec	532 MB/sec	532 MB/sec	532 MB/sec	532 MB/sec	2000 MB/sec	2000 MB/sec	400 MB/sec	400 MB/sec
NOR FLASH	32 MB	8 M	8 M	8 M	8 M	8 M	16 M	16 M	16 M	2 M
Max NAND FLASH	---	1 GB	512 MB	512 MB	256 MB	256 MB	None	None	None	None
Max FPGA RAM	512 MB	---	N/A	N/A	N/A	N/A	64 M	64 M	32 M[1]	8 M[1]
FPGA RAM Throughput	TBD	---	N/A	N/A	N/A	N/A	400 MB/sec	400 MB/sec	400 MB/sec	400 MB/sec
Interface	**MXM 3.0 Type**	**SO-DIMM-204**	**SO-DIMM-200**	**SO-DIMM-200**	**SO-DIMM-200**	**SO-DIMM-200**	**SO-DIMM-200**	**SO-DIMM-200**	**SO-DIMM-144**	**SO-DIMM-144**
Required Voltages	5	3.3 - 5	3.3	3.3	3.3	3.3	3.3	3.3	3.3, 2.5, 1.23	3.3, 2.5, 1.23
Avail FPGA I/O	107	---	96	88	96	96	140	140	100	100
Peripherals										
Ethernet MAC	2 x 10/100/1000	2 x 10/100/1000	10/100	10/100	10/100	10/100	10/100/1000	10/100/1000	0[3]	0[3]
McBSP Ports	N/A	N/A	2	2	2	2	2	2	2	2
LCD	1	1	1	1	1	1	N/A	N/A	0[2]	0[2]
VPIF	N/A	N/A	1	1	1	1	N/A	N/A	N/A	N/A
MMC/SD	1	3	1	1	1	1	0[6]	0[6]	0[6]	0[6]
SATA	1	N/A	1	1	1	1	N/A	N/A	N/A	N/A
I2C	4	2	2[6]	2[6]	2[6]	2[6]	1[6]	1[6]	0[6]	0[6]
SPI	2	2	2[6]	2[6]	2[6]	2[6]	0[6]	0[6]	0[6]	0[6]
USB	2	2	2	2	2	2	0[6]	0[6]	0[6]	0[6]
UARTS	2	6	3[6]	3[6]	3[6]	3[6]	1[6]	1[6]	1[6]	1[6]
CAN	2	2	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
PCIe	PCIe x4	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Transceivers	6 x 3.125 Gbps	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Availability	**In Production**	**In Production**	**In Production**	**In Production**	**In Production**	**In Production**	**In Production**	**In Production**	**In Production**	**In Production**
Introduction Date	**2013**	**2012**	**2010**	**2010**	**2010**	**2010**	**2006**	**2006**	**2004**	**2004**

Notes:

1. FPGA and CPU share RAM via DSP EMIF, 100 MHz clock rate maximum.
2. LCD interface core is available for the FPGA to drive local and remote LCD display.
3. Soft FPGA MAC cores are available for 10/100 Mbit Ethernet Phy Control.
4. Spartan-6 features a 6 input LUT allowing for significantly more logic in the same number of slices when compared to a Spartan-3.
5. TMS6455 Option Including 8 Rocket I/O ports is available upon request.
6. The listed peripheral interfaces are available from the DSP/ARM. Additional interfaces can be created in modules with FPGA's.
7. These modules are available with or without the FPGA.