BURR-BROWN®

PCM54
PCM55

DESIGNED FOR AUDIO

16-Bit Monolithic DIGITAL-TO-ANALOG CONVERTERS

FEATURES

- **PARALLEL INPUT FORMAT**
- **16-BIT RESOLUTION**
- **15-BIT MONOTONICITY (typ)**
- **–92dB TOTAL HARMONIC DISTORTION (K Grade)**
- **3μs SETTLING TIME (Voltage Out)**
- **96dB DYNAMIC RANGE**
- **±3V or ±1mA AUDIO OUTPUT**
- **OPERATES ON ±5V (PCM55) TO ±12V (PCM54) SUPPLIES**
- **28-PIN DIP (PCM54)**
- **24-LEAD SOIC (PCM55)**

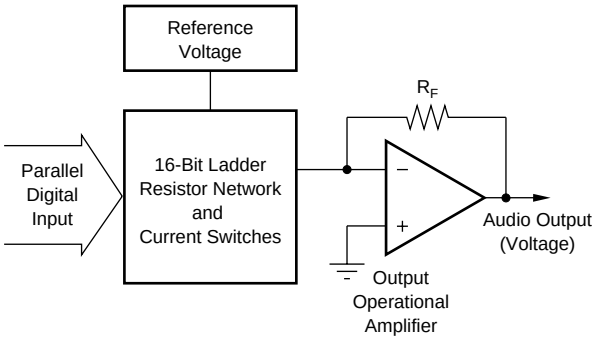
DESCRIPTION

The PCM54 and PCM55 family of converters are parallel input, fully monotonic, 16-bit digital-to-analog converters that are designed and specified for digital audio applications. These devices employ ultra-stable nichrome (NiCr) thin-film resistors to provide monotonicity, low distortion, and low differential linearity error (especially around bipolar zero) over long periods of time and over the full operating temperature.

These converters are completely self-contained with a stable, low noise, internal, zener voltage reference; high speed current switches; a resistor ladder network; and a fast settling, low noise output operational amplifier all on a single monolithic chip. The converters are operated using two power supplies that can range from ±5V (PCM55) to ±12V (PCM54). Power dissipation with ±5V supplies is typically less than 200mW. Also included is a provision for external adjustment of the MSB error (differential linearity error at bipolar zero, PCM54 only) to further improve Total Harmonic Distortion (THD) specifications if desired.

A current output (I_{OUT}) wiring option is provided. This output typically settles to within ±0.006% of FSR final value in 350ns (in response to a full-scale change in the digital input code).

The PCM54 is packaged in 28-pin plastic DIP package. The PCM55 is available in a 24-lead plastic miniflatpak.



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SPECIFICATIONS

ELECTRICAL

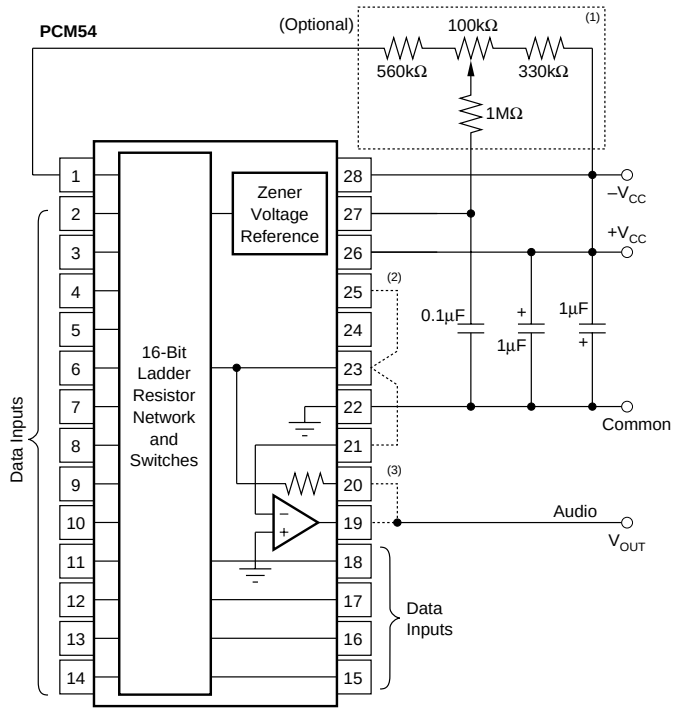
At +25°C and $\pm V_{CC}$ = 12V, unless otherwise noted.

PARAMETER	PCM54HP, PCM55HP MIN	PCM54HP, PCM55HP TYP	PCM54HP, PCM55HP MAX	PCM54JP, PCM55JP MIN	PCM54JP, PCM55JP TYP	PCM54JP, PCM55JP MAX	PCM54KP MIN	PCM54KP TYP	PCM54KP MAX	UNITS
DIGITAL INPUTS										
Resolution		16			✻			✻		Bits
Dynamic Range		96			✻			✻		dB
Logic Levels (TTL/CMOS Compatible):										
V_{IH}	+2.4		+5.25	✻		✻	✻		✻	V
V_{IL}	0		+0.8	✻		✻	✻		✻	V
I_{IH}, V_{IN} = +2.7V			+40			✻			✻	µA
I_{IL}, V_{IN} = +0.4V			–0.5			✻			✻	mA
TRANSFER CHARACTERISTICS										
ACCURACY										
Gain Error		±2			✻			✻		%
Bipolar Zero Error		±30			✻			✻		mV
Differential Linearity Error at Biploar Zero[1]		±0.001			✻			✻		% FSR[2]
Noise (rms) (20Hz to 20kHz) at Bipolar Zero		12			✻			✻		µV
TOTAL HARMONIC DISTORTION[3]										
(16-Bit Resolution)										
V_O = ±FS at f = 991Hz		–94	–82		✻	–88	✻	✻	–92	dB
V_O = –20dB at f = 991Hz		–74	–68		✻	✻	✻	–80	–74	dB
V_O = –60dB at f = 991Hz		–34	–28		✻	✻	✻	–40	–34	dB
MONOTONICITY		15			✻			✻		Bits
SETTLING TIME (to ±0.006% of FSR)										
Voltage Output: 6V Step		3			✻			✻		µs
1LSB Step		1			✻			✻		µs
Current Output (1mA Step): 10Ω to 100Ω Load		350			✻			✻		ns
1kΩ Load[4]		350			✻			✻		ns
Deglitcher Delay (THD Test)[5]		2.5	4		✻	✻		✻	✻	µs
Slew Rate		10			✻			✻		V/µs
WARM-UP TIME	1			✻			✻			Min
ANALOG OUTPUT										
Voltage Output: Bipolar Range		±3			✻			✻		V
Output Current	±2			✻			✻			mA
Output Impedance		0.1			✻			✻		Ω
Short-Circuit Duration		Indefinite to Common			✻			✻		
Current Output:[6]										
Bipolar Range (±30%)		±1			✻			✻		mA
Bipolar Output Impedance (±30%)		1.2			✻			✻		kΩ
POWER SUPPLY REQUIREMENTS										
Voltage: $+V_{CC}$ (PCM54)	+4.75	+12	+15.75	✻	✻	✻	✻	✻	✻	V
$–V_{CC}$ (PCM54)	–4.75	–12	–15.75	✻	✻	✻	✻	✻	✻	V
$+V_{CC}$ (PCM55)	+4.75	+5	+7.5	✻	✻	✻	✻	✻	✻	V
$–V_{CC}$ (PCM55)	–4.75	–5	–7.5	✻	✻	✻	✻	✻	✻	V
Supply Drain: $+V_{CC}$		+13	+20		✻	✻		✻	✻	mA
$–V_{CC}$		–16	–25		✻	✻		✻	✻	mA
TEMPERATURE RANGE										
Operating	0		+70	✻		✻	✻		✻	°C
Storage	–55		+100	✻		✻	✻		✻	°C

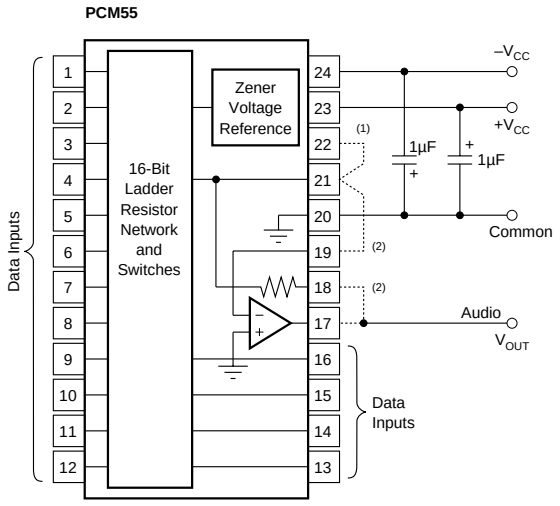
✻ Specifications same as for PCM54HP.

NOTES: (1) Externally adjustable. If external adjustment is not used, connect a 0.01µF capacitor to Common to reduce noise pickup. (2) FSR means Full-Scale Range and is 6V for ±3V output. (3) The measurement of total harmonic distortion is highly dependent on the characteristics of the measurement circuit. Burr-Brown may calculate THD from the measured linearity errors using Equation 2 in the section on "Total Harmonic Distortion," but specifies that the maximum THD measured with the circuit shown in Figure 2 will be less than the limits indicated. (4) Measured with an active clamp to provide a low impedance for approximately 200ns. (5) Deglitcher or sample/hold delay used in THD measurement test circuit. See Figures 2 and 3. (6) Output amplifier disconnected.

CONNECTION DIAGRAMS



NOTES: (1) MSB error (BPZ differential linearity error) can be adjusted to zero using this external circuit. (2) Connect to bipolar operation ($+V_{CC} \geq 8.5V$ for unipolar operation). (3) Connect for V_{OUT} operation. When V_{OUT} amp is not being used (I_{OUT} mode), terminate with an external 3kΩ feedback resistor between pin 19 and pin 21, and a 1kΩ resistor between pin 21 and pin 22 to reduce possible noise effects.



NOTES: (1) Connect for bipolar operation. ($+V_{CC} \geq 8.5V$ for unipolar operation.) (2) Connect for V_{OUT} operation. When V_{OUT} amp is not being used (I_{OUT} mode), terminate with an external 3kΩ feedback resistor between pin 17 and pin 19, and a 1kΩ resistor between pin 19 and pin 20 to reduce possible noise effects.

PIN ASSIGNMENTS

PIN	PCM54-DIP	PIN	PCM54-DIP
1	Trim	15	Bit 13
2	Bit 1 (MSB)	16	Bit 14
3	Bit 2	17	Bit 15
4	NC	18	Bit 16 (LSB)
5	Bit 3	19	V_{OUT}
6	Bit 4	20	R_{FB}
7	Bit 5	21	SJ
8	Bit 6	22	Common
9	Bit 7	23	I_{OUT}
10	Bit 8	24	NC
11	Bit 9	25	I_{BPO}
12	Bit 10	26	$+V_{CC}$
13	Bit 11	27	MSB Adjust
14	Bit 12	28	$-V_{CC}$

PIN ASSIGNMENTS

PIN	PCM55-SOIC	PIN	PCM55-SOIC
1	Bit 1 (MSB)	13	Bit 13
2	Bit 2	14	Bit 14
3	Bit 3	15	Bit 15
4	Bit 4	16	Bit 16
5	Bit 5	17	V_{OUT}
6	Bit 6	18	Feedback Resistor
7	Bit 7	19	Summing Junction
8	Bit 8	20	Common
9	Bit 9	21	Current Output
10	Bit 10	22	Bipolar Offset
11	Bit 11	23	$+V_{CC}$
12	Bit 12	24	$-V_{CC}$

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
PCM54HP	28-Pin DIP	215
PCM54JP	28-Pin DIP	215
PCM54KP	28-Pin DIP	215
PCM55HP	24-Lead SOIC	178
PCM55JP	24-Lead SOIC	178

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	±18VDC
Input Logic Voltage	–1V to +5.5V
Power Dissipation	PCM54 800mW, PCM55 400mW
Storage Temperature	–55°C to +100°C
Lead Temperature, (soldering, 10s)	+300°C

ORDERING INFORMATION

PRODUCT	THD at FS	PACKAGE
PCM54HP	0.008	28-Pin DIP
PCM54JP	0.004	28-Pin DIP
PCM54KP	0.0025	28-Pin DIP
PCM55HP	0.008	24-Lead SOIC
PCM55JP	0.004	24-Lead SOIC

DISCUSSION OF SPECIFICATIONS

The PCM54 and PCM55 are specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for a D/A converter in audio applications are total harmonic distortion, differential linearity error, bipolar zero error, parameter shifts with time and temperature, and settling time effects on accuracy.

The PCM54 and PCM55 are factory-trimmed and tested for all critical key specifications.

The accuracy of a D/A converter is described by the transfer function shown in Figure 1. Digital input to analog output relationship is shown in Table I. The errors in the D/A converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including gain, offset, linearity, differential linearity, and power supply sensitivity. Gain drift over temperature rotates the line (Figure 1) about the bipolar zero point and offset drift shifts the line left or right over the operating temperature range. Most of the offset and gain drift with temperature or time is due to the drift of the internal reference zener diode. The converter is designed so that these drifts are in opposite directions. This way, the bipolar zero voltage is virtually unaffected by variations in the reference voltage.

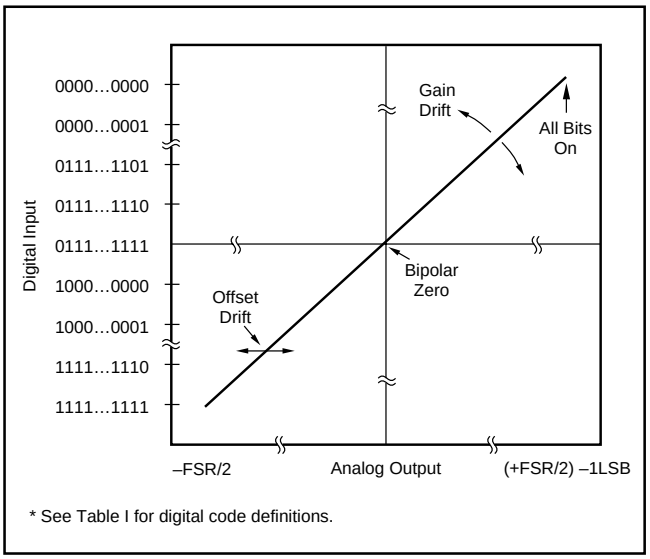


FIGURE 1. Input vs Output for an Ideal Bipolar D/A Converter.

DIGITAL INPUT CODES

The PCM54 and PCM55 accept complementary digital input codes in any of three binary formats (CSB, unipolar; or COB, bipolar; or CTC, Complementary Two's Complement, bipolar). See Table II.

Digital Input Codes	ANALOG OUTPUT		
	Complementary Straight Binary (CSB)	Complementary Offset Binary (COB)	Complementary Two's Complement (CTS)[1]
0000_H	+Full Scale	+Full Scale	–1LSB
$7FFF_H$	+1/2 Full Scale	Bipolar Zero	–Full Scale
8000_H	+1/2 Full Scale –1LSB	–1LSB	+Full Scale
$FFFF_H$	Zero	–Full Scale	Bipolar Zero

NOTE: (1) Invert the MSB of the COB code with an external inverter to obtain CTC code.

TABLE II. Digital Input Codes.

BIPOLAR ZERO ERROR

Initial Bipolar Zero (BPZ) error (Bit 1 "ON" and all other bits "OFF") is the deviation from 0V out and is factory-trimmed to typically ±10mV at +25°C.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from an ideal 1LSB change from one adjacent output state to the next. DLE is important in audio applications because excessive DLE at bipolar zero (at the "major carry") can result in audible crossover distortion for low level output signals. Initial DLE on the PCM54 and PCM55 is factory-trimmed to typically ±0.001% of FSR. This error is adjustable to zero using the circuit shown in the connection diagram (PCM54 only).

VOLTAGE OUTPUT MODE							
		Analog Output					
		Unipolar[1]			Bipolar		
Digital Input Code		16-Bit	15-Bit	14-Bit	16-Bit	15-Bit	14-Bit
One LSB	(µV)	91.6	183	366	91.6	183	366
0000_H	(V)	+5.99991	+5.99982	+5.99963	+2.99991	+2.99982	+2.99963
$FFFF_H$	(V)	0	0	0	–3.0000	–3.0000	–3.0000
CURRENT OUTPUT MODE							
		Analog Output					
		Unipolar			Bipolar		
Digital Input Code		16-Bit	15-Bit	14-Bit	16-Bit	15-Bit	14-Bit
One LSB	(µA)	0.031	0.061	0.122	0.031	0.061	0.122
0000_H	(mA)	–1.99997	–1.99994	–1.99988	–0.99997	–0.99994	–0.99988
$FFFF_H$	(mA)	0	0	0	+1.00000	+1.00000	+1.00000

NOTE: (1) $+V_{CC}$ must be at least +8.5VDC to allow output to swing to +6.0VDC.

TABLE I. Digital Input to Analog Output Relationship.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy.

The PCM54 and PCM55 power supply sensitivity is shown by Figure 2. Normally, regulated power supplies with 1% or less ripple are recommended for use with the DAC. See also Power Supply Connections paragraph in the Installation and Operating Instructions section.

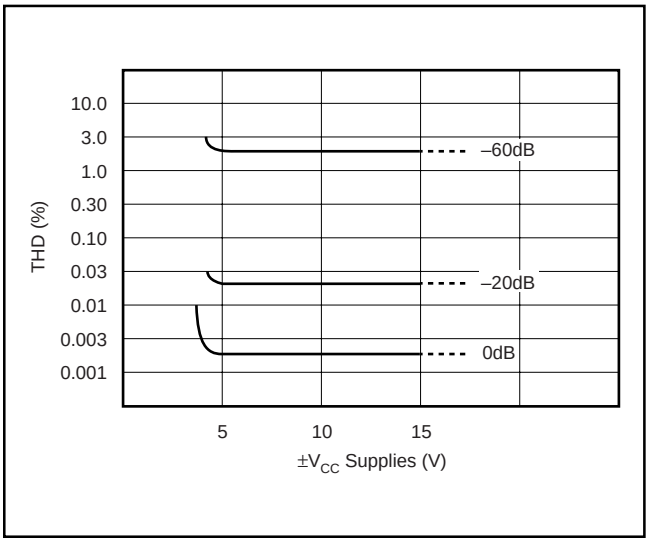


FIGURE 2. Effects of $\pm V_{CC}$ on Total Harmonic Distortion (PCM54JP; V_{CC}s with approximately 2% ripple).

SETTLING TIME

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 3).

Settling times are specified to ±0.006% of FSR; one for a large output voltage change of 3V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111…11 to 10000.00), the point at which the worst-case settling time occurs.

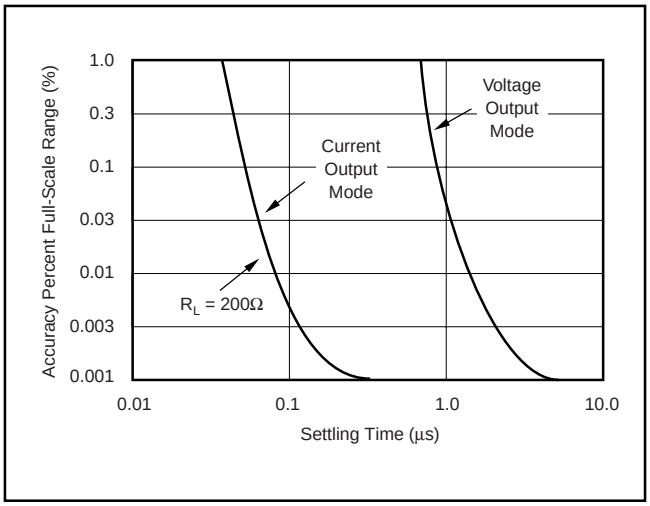


FIGURE 3. Full-Scale Range Settling Time vs Accuracy.

STABILITY WITH TIME AND TEMPERATURE

The parameters of a D/A converter designed for audio applications should be stable over a relatively wide temperature range and over long periods of time to avoid undesirable periodic readjustment. The most important parameters are bipolar zero, differential linearity error, and total harmonic distortion. Most of the offset and gain drift with temperature or time is due to the drift of the internal reference zener diode. The PCM54 and PCM55 are designed so that these drifts are in opposite directions so that the bipolar zero voltage is virtually unaffected by variations in the reference voltage. Both DLE and THD are dependent upon the matching and tracking of resistor ratios and upon V_{BE} and h_{FE} of the current-source transistors. The PCM54 and PCM55 were designed so that any absolute shift in these components has virtually no effect on DLE or THD. The resistors are made of identical links of ultra-stable nichrome thin-film. The current density in these resistors is very low to further enhance their stability.

DYNAMIC RANGE

The dynamic range is a measure of the ratio of the smallest signals the converter can produce to the full-scale range and is usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6 x n, or about 96dB for a 16-bit converter. The actual, or useful, dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit. However, this does point out that a resolution of at least 16 bits is required to obtain a 90dB minimum dynamic range, regardless of the accuracy of the converter. Another specification that is useful for audio applications is total harmonic distortion.

TOTAL HARMONIC DISTORTION

THD is useful in audio applications and is a measure of the magnitude and distribution of the linearity error, differential linearity error, and noise as well as quantization error. To be useful, THD should be specified for both high level and low level input signals. This error is unadjustable and is the most meaningful indicator of D/A converter accuracy for audio applications.

The THD is defined as the ratio of the square root of the sum of the squares of the values of the harmonics to the value of the fundamental input frequency and is expressed in percent or dB. The rms value of the PCM54/55 error referred to the input can be shown to be:

(1)

$$\varepsilon_{rms} = \sqrt{\frac{1}{n} \sum_{i=1}^{n} [E_L(i) + E_Q(i)]^2}$$

where n is the number of samples in one cycle of any given sine wave, $E_L(i)$ is the linearity error of the PCM54 or PCM55 at each sampling point, and $E_Q(i)$ is the quantization

error at each sampling point. The THD can then be expressed as:

(2)

$$THD = \frac{\varepsilon_{rms}}{E_{rms}} = \sqrt{\frac{\frac{1}{n}\sum_{i=1}^{n}[E_L(i) + E_Q(i)]^2}{E_{rms}}} \cdot 100\%$$

where E_{rms} is the rms signal voltage level.

This expression indicates that, in general, there is a correlation between the THD and the square root of the sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to the THD.

For PCM54/55 the test period was chosen to be 22.7µs (44.1kHz) which is compatible with the EIAJ STC-007 specification for PCM audio. The test frequency is 420Hz and the amplitude of the input signal is 0dB, –20dB, and –60dB down from full scale.

Figure 4 shows the typical THD as a function of output voltage.

Figure 5 shows typical THD as a function of frequency.

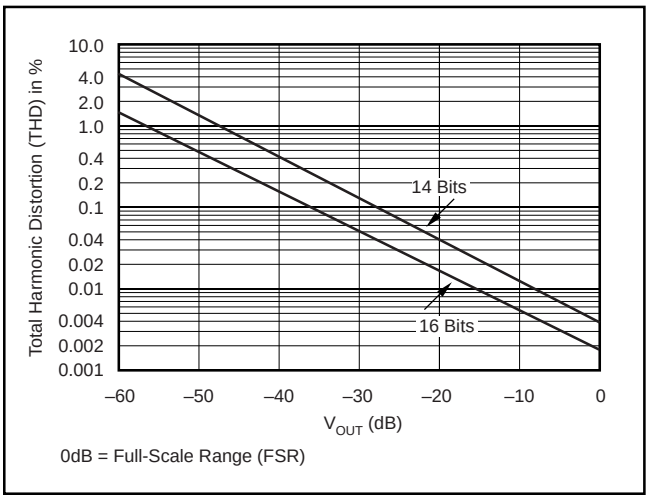


FIGURE 4. Total Harmonic Distortion (THD) vs V_{OUT}.

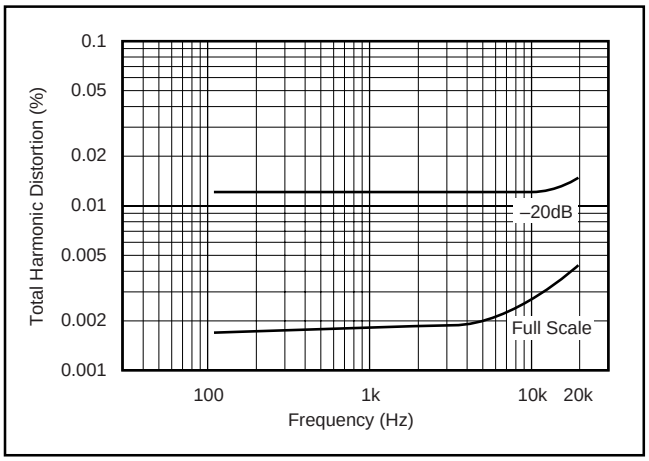


FIGURE 5. Total Harmonic Distortion (THD) vs Frequency.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the connections diagram. These capacitors (1µF tantalum or electrolytic recommended) should be located close to the converter.

MSB ERROR ADJUSTMENT PROCEDURE (OPTIONAL)

The MSB error of the PCM54 and PCM55 can be adjusted to make the differential linearity error (DLE) at BPZ essentially zero. This is important when the signal output levels are very low because zero crossing noise (DLE at BPZ) becomes very significant when compared to the small code changes occurring in the LSB portion of the converter.

Differential linearity error at bipolar zero is guaranteed to meet data sheet specifications without any external adjustment. However, a provision has been made for an optional adjustment of the MSB linearity point which makes it possible to eliminate DLE error at BPZ (PCM54 only). Two procedures are given to allow either static or dynamic adjustment. The dynamic procedure is preferred because of the difficulty associated with the static method (accurately measuring 16-bit LSB steps).

To statically adjust DLE at BPZ, refer to the circuit shown in Figure 6 or the PCM54 connection diagram. After allowing ample warm-up time (20-30 minutes) to assure stable operation of the PCM54, select input code 8000 hexadecimal (all bits off except the MSB). Measure and record it. Change the digital input code to 7FFF hexadecimal (all bits off except the MSB). Adjust the 100kΩ potentiometer to make the audio output read 92µV more than the voltage reading of the previous code (a ILSB step = 92µV).

A much simpler method is to dynamically adjust the DLE at BPZ. Again, refer to Figure 6 or the PCM54 connection diagram for circuitry and component values. Assuming the device has been installed in a digital audio application circuit, send the appropriate digital input to produce a –60dB level sinusoidal output. While measuring the THD of the audio circuit output, adjust the 100kΩ potentiometer until a minimum level of distortion is observed.

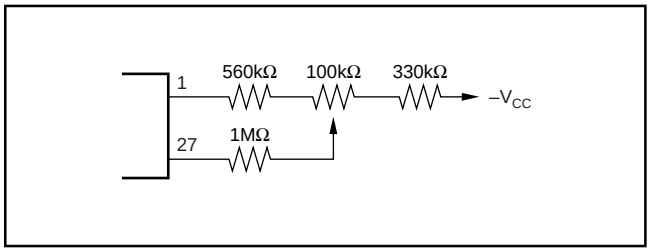


FIGURE 6. MSB Differential Linearity at Bipolar Zero Adjustment Circuit (optional).

INSTALLATION CONSIDERATIONS

If the optional external MSB error circuitry is used (PCM54), a potentiometer with adequate resolution and a TCR of 100ppm/°C or less is required. Also, extra care must be taken to insure that no leakage path (either AC or DC) exists to pin 27 (PCM54). If circuit is not used, pin 1 (PCM54) should be terminated to common with a 0.01µF capacitor.

The PCM converter and the wiring to its connectors should be located to provide the optimum isolation from sources of RFI and EMI. The important consideration in the elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together, they represent a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

APPLICATIONS

A sample/hold amplifier, or "deglitcher", is required at the output of the D/A converter for both the left and right channel, as shown in Figure 7. The S/H amplifier for the left channel is composed of A_2, SW_1, and associated circuitry. A_2 is used as an integrator to hold the analog voltage in C_1. Since the source and drain of the FET switch operates at a virtual ground when "C" and "B" are closed in the simple mode, there is no increase in distortion caused by the modulation effect of R_{ON} by the audio signal.

Figure 8 shows the deglitcher control signals for both the left and right channels which are produced by the timing control logic. A delay of 2.5µs (tω) is provided to eliminate the glitch and allow the output of the PCM54-V to settle within a small error band around its final value before connecting it to the channel output.

Due to the fast settling time of the PCM54-V, it is possible to minimize the delay between the left channel and right channel outputs when using a single D/A converter for both channels. This is important because the left and right channel data is recorded in phase and use of a slower D/A converter would result in significant phase error at the higher audio frequencies.

A low-pass filter is required at the S/H output to remove all unwanted frequency components caused by the sampling frequency as well as the discrete nature of the D/A converter output. The filter must have a flat amplitude response over the entire audio band (0 to 20kHz) and a very high attenuation above 20kHz. Most previous digital audio circuits used a high-order (9-13 pole) analog filter. However, the phase response of an analog filter with these amplitude characteristics is nonlinear and can disturb the pulse-shaped characteristics of the transients contained in music.

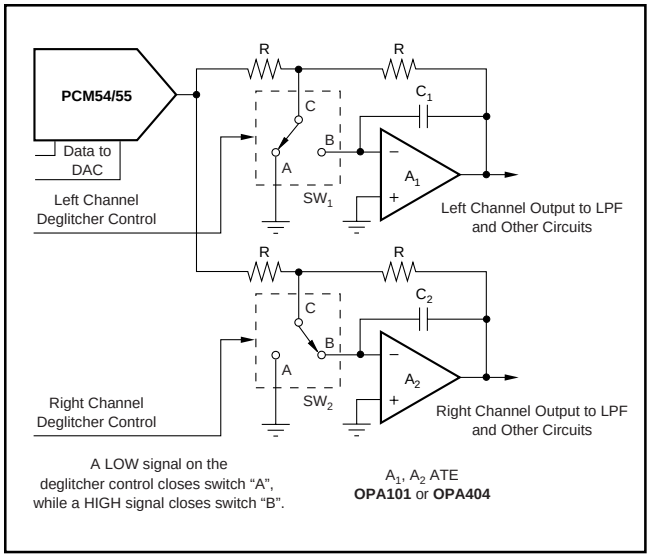
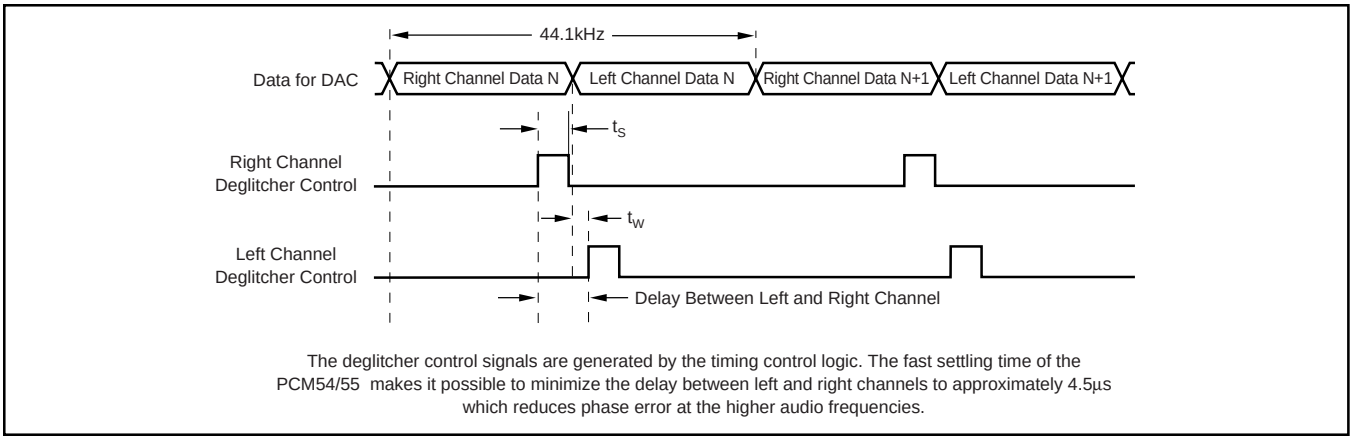


FIGURE 7. A Sample/Hold Amplifier (deglitcher) is Required at the Digital-to-Analog Output for Both Left and Right Channels.



The deglitcher control signals are generated by the timing control logic. The fast settling time of the PCM54/55 makes it possible to minimize the delay between left and right channels to approximately 4.5µs which reduces phase error at the higher audio frequencies.

FIGURE 8. Timing Diagram for the Deglitcher Control Signals.