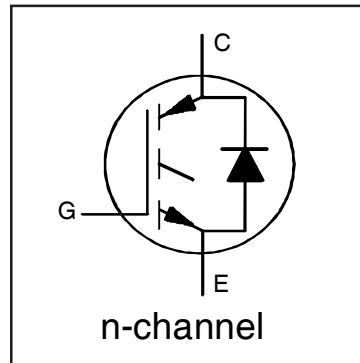


**INSULATED GATE BIPOLAR TRANSISTOR WITH ULTRA-LOW VF DIODE
FOR INDUCTION HEATING AND SOFT SWITCHING APPLICATIONS**

IRGP4068DPbF IRGP4068D-EPbF

Features

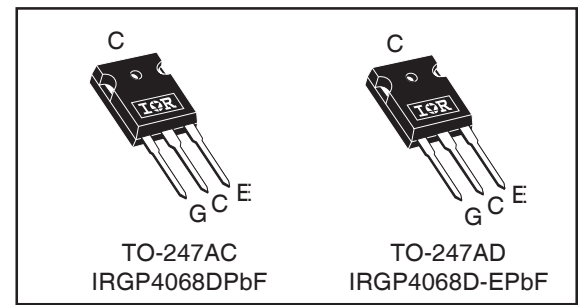
- Low $V_{CE(ON)}$ Trench IGBT Technology
- Low Switching Losses
- Maximum Junction temperature 175 °C
- 5 μ S short circuit SOA
- Square RBSOA
- 100% of the parts tested for 4X rated current (I_{LM})
- Positive $V_{CE(ON)}$ Temperature co-efficient
- Ultra-low V_F Hyperfast Diode
- Tight parameter distribution
- Lead Free Package



$V_{CES} = 600V$
$I_C = 48A, T_C = 100^\circ C$
$t_{SC} \geq 5\mu s, T_{J(max)} = 175^\circ C$
$V_{CE(on)} \text{ typ.} = 1.65V$

Benefits

- Device optimized for induction heating and soft switching applications
- High Efficiency due to Low $V_{CE(on)}$, Low Switching Losses and Ultra-low V_F
- Rugged transient Performance for increased reliability
- Excellent Current sharing in parallel operation
- Low EMI



G	C	E
Gate	Collector	Emitter

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage	600	V
$I_C @ T_C = 25^\circ C$	Continuous Collector Current	96	A
$I_C @ T_C = 100^\circ C$	Continuous Collector Current	48	
I_{CM}	Pulse Collector Current	192	
I_{LM}	Clamped Inductive Load Current ①	192	
$I_F @ T_C = 160^\circ C$	Diode Continuous Forward Current	8.0	
I_{FSM}	Diode Non Repetitive Peak Surge Current @ $T_J = 25^\circ C$ ②	175	
I_{FM}	Diode Peak Repetitive Forward Current ②	16	V
V_{GE}	Continuous Gate-to-Emitter Voltage	± 20	
	Transient Gate-to-Emitter Voltage	± 30	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	330	W
$P_D @ T_C = 100^\circ C$	Maximum Power Dissipation	170	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Mounting Torque, 6-32 or M3 Screw	10 lbf-in (1.1 N·m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$ (IGBT)	Thermal Resistance Junction-to-Case-(each IGBT)	—	—	0.45	°C/W
$R_{\theta JC}$ (Diode)	Thermal Resistance Junction-to-Case-(each Diode)	—	—	2.0	
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink (flat, greased surface)	—	0.24	—	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (typical socket mount)	—	80	—	

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	Ref.Fig
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	$V_{GE} = 0V, I_C = 100\mu A$ ③	CT6
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.30	—	V/°C	$V_{GE} = 0V, I_C = 1mA$ (25°C-175°C)	CT6
$V_{CE(on)}$	Collector-to-Emitter Saturation Voltage	—	1.65	2.14	V	$I_C = 48A, V_{GE} = 15V, T_J = 25^\circ\text{C}$	4,5,6
		—	2.0	—		$I_C = 48A, V_{GE} = 15V, T_J = 150^\circ\text{C}$	8,9,10
		—	2.05	—		$I_C = 48A, V_{GE} = 15V, T_J = 175^\circ\text{C}$	
$V_{GE(th)}$	Gate Threshold Voltage	4.0	—	6.5	V	$V_{CE} = V_{GE}, I_C = 1.4mA$	8,9
$\Delta V_{GE(th)}/\Delta T_J$	Threshold Voltage temp. coefficient	—	-21	—	mV/°C	$V_{CE} = V_{GE}, I_C = 1.0mA$ (25°C - 175°C)	10,11
g_{fe}	Forward Transconductance	—	32	—	S	$V_{CE} = 50V, I_C = 48A, PW = 80\mu s$	
I_{CES}	Collector-to-Emitter Leakage Current	—	1.0	150	μA	$V_{GE} = 0V, V_{CE} = 600V$	
		—	450	1000		$V_{GE} = 0V, V_{CE} = 600V, T_J = 175^\circ\text{C}$	
V_{FM}	Diode Forward Voltage Drop	—	0.96	1.05	V	$I_F = 8.0A$	7
		—	0.81	0.86		$I_F = 8.0A, T_J = 150^\circ\text{C}$	
I_{GES}	Gate-to-Emitter Leakage Current	—	—	± 100	nA	$V_{GE} = \pm 20V$	

Switching Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions	Ref.Fig
Q_g	Total Gate Charge (turn-on)	—	95	140	nC	$I_C = 48A$ $V_{GE} = 15V$ $V_{CC} = 400V$	18 CT1
Q_{ge}	Gate-to-Emitter Charge (turn-on)	—	28	42			
Q_{gc}	Gate-to-Collector Charge (turn-on)	—	35	53			
E_{off}	Turn-Off Switching Loss	—	1275	1481	μJ	$I_C = 48A, V_{CC} = 400V, V_{GE} = 15V$ $R_G = 10\Omega, L = 200\mu H, T_J = 25^\circ\text{C}$ Energy losses include tail	CT4
$t_{d(off)}$	Turn-Off delay time	—	145	176	μJ	$I_C = 48A, V_{CC} = 400V, V_{GE} = 15V$ $R_G = 10\Omega, L = 200\mu H, T_J = 25^\circ\text{C}$	
t_f	Fall time	—	35	46			
E_{off}	Turn-Off Switching Loss	—	1585	—	μJ	$I_C = 48A, V_{CC} = 400V, V_{GE} = 15V$ $R_G = 10\Omega, L = 200\mu H, T_J = 175^\circ\text{C}$ Energy losses include tail	CT4
$t_{d(off)}$	Turn-Off delay time	—	165	—	μJ	$I_C = 48A, V_{CC} = 400V, V_{GE} = 15V$ $R_G = 10\Omega, L = 200\mu H, T_J = 175^\circ\text{C}$	WF1
t_f	Fall time	—	45	—			
C_{ies}	Input Capacitance	—	3025	—	pF	$V_{GE} = 0V$ $V_{CC} = 30V$ $f = 1.0Mhz$	17
C_{oes}	Output Capacitance	—	245	—			
C_{res}	Reverse Transfer Capacitance	—	90	—			
RBSOA	Reverse Bias Safe Operating Area	FULL SQUARE				$T_J = 175^\circ\text{C}, I_C = 192A$ $V_{CC} = 480V, V_p = 600V$ $R_g = 10\Omega, V_{GE} = +15V$ to 0V	3 CT2
SCSOA	Short Circuit Safe Operating Area	5	—	—	μs	$V_{CC} = 400V, V_p = 600V$ $R_g = 10\Omega, V_{GE} = +15V$ to 0V	16, CT3 WF2

Notes:

- ① $V_{CC} = 80\% (V_{CES}), V_{GE} = 20V, L = 200\mu H, R_G = 10\Omega$.
- ② Pulse width limited by max. junction temperature.
- ③ Refer to AN-1086 for guidelines for measuring $V_{(BR)CES}$ safely.

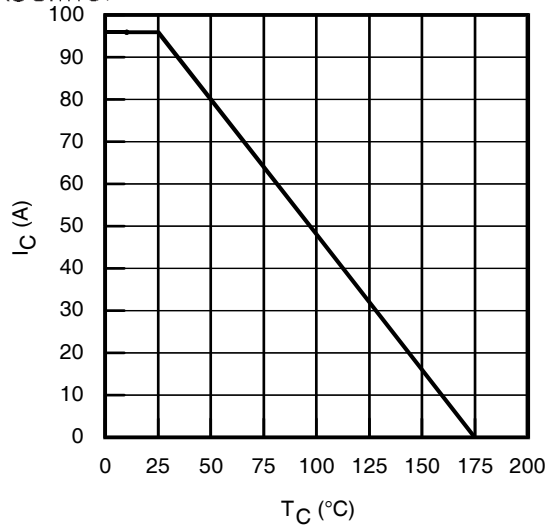


Fig. 1 - Maximum DC Collector Current vs. Case Temperature

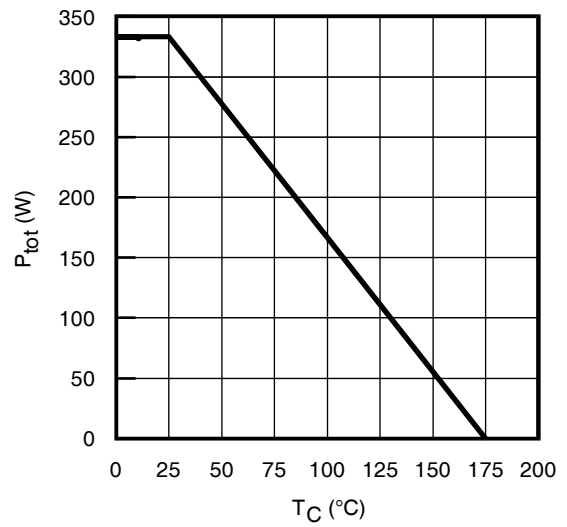


Fig. 2 - Power Dissipation vs. Case Temperature

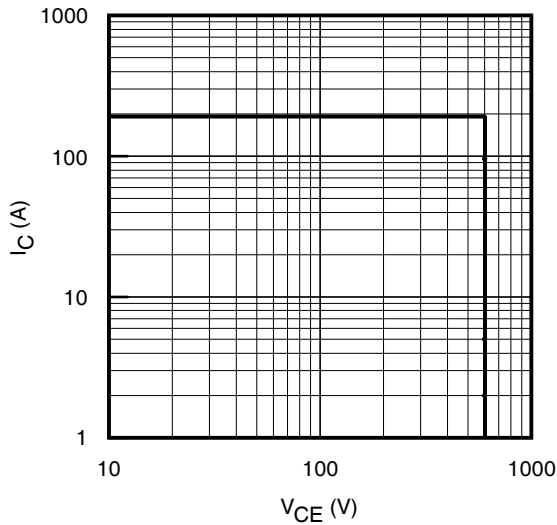


Fig. 3 - Reverse Bias SOA
 $T_J = 175^{\circ}C$; $V_{GE} = 15V$

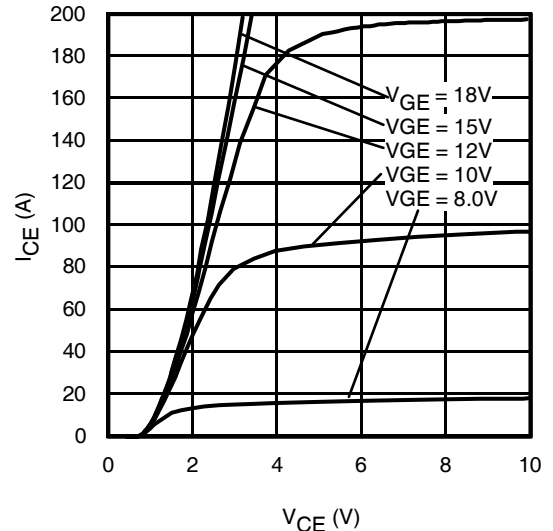


Fig. 4 - Typ. IGBT Output Characteristics
 $T_J = -40^{\circ}C$; $t_p = 80\mu s$

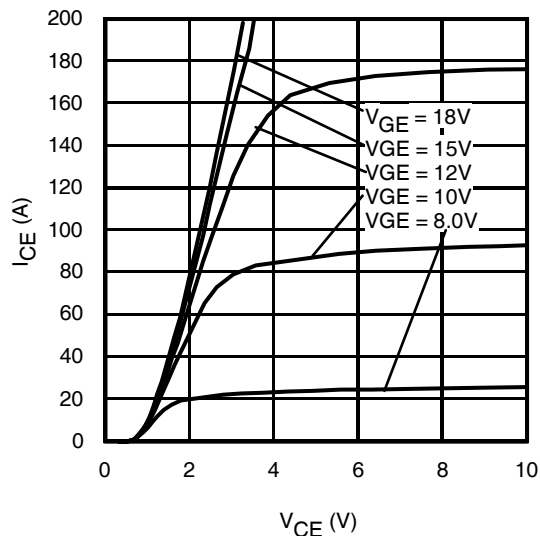


Fig. 5 - Typ. IGBT Output Characteristics
 $T_J = 25^{\circ}C$; $t_p = 80\mu s$

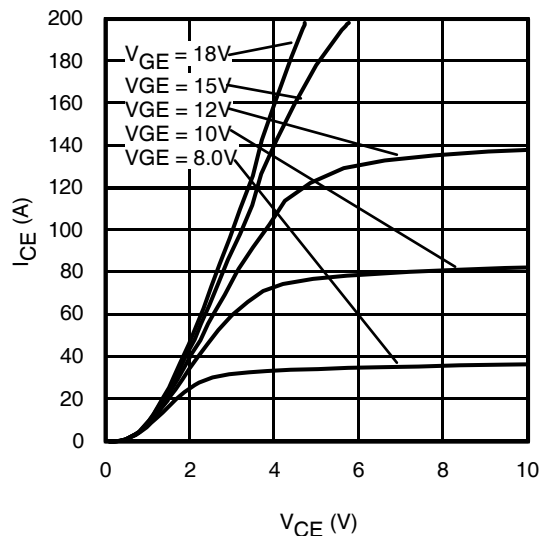


Fig. 6 - Typ. IGBT Output Characteristics
 $T_J = 175^{\circ}C$; $t_p = 80\mu s$

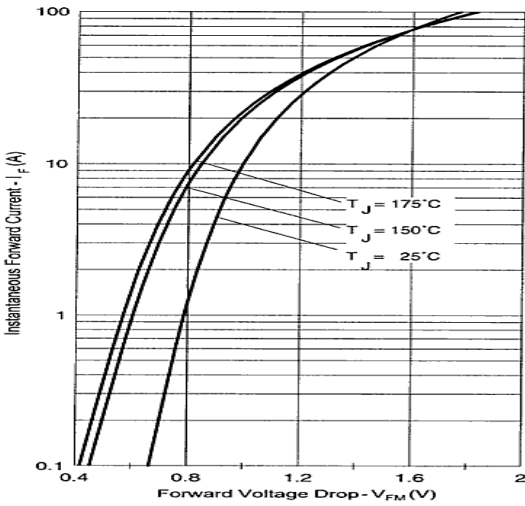
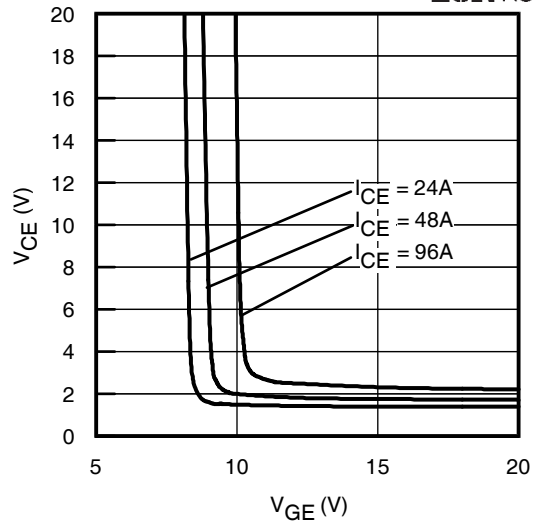
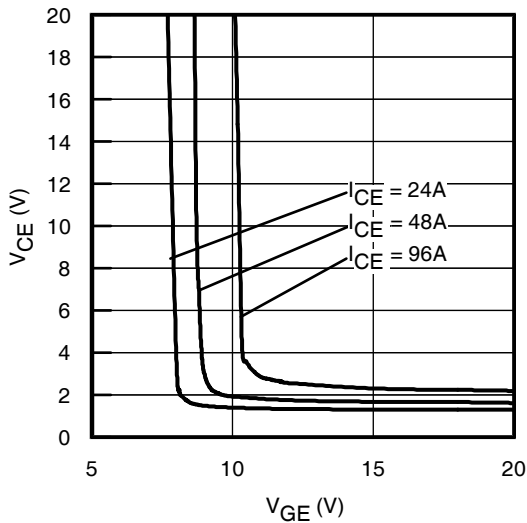


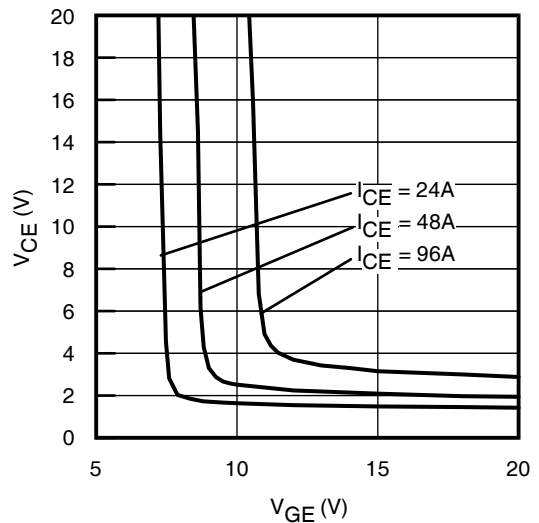
Fig. 7 - Typ. Diode Forward Voltage Drop Characteristics



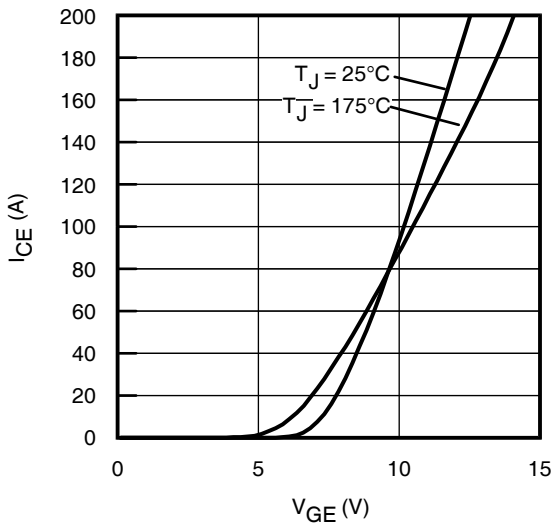
**Fig. 8 - Typical V_{CE} vs. V_{GE}
 $T_J = -40^\circ\text{C}$**



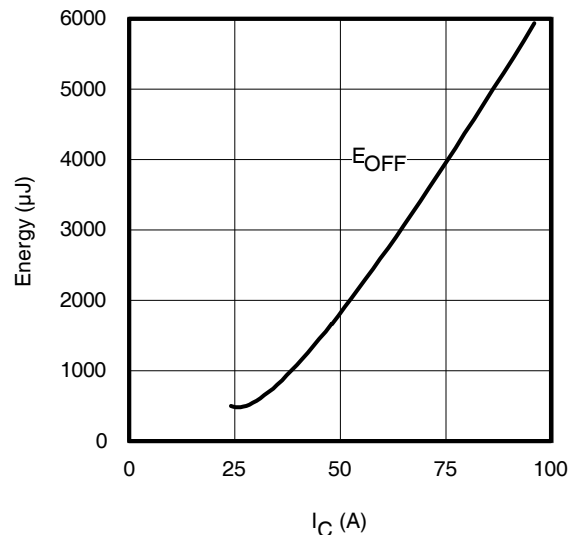
**Fig. 9 - Typical V_{CE} vs. V_{GE}
 $T_J = 25^\circ\text{C}$**



**Fig. 10 - Typical V_{CE} vs. V_{GE}
 $T_J = 175^\circ\text{C}$**



**Fig. 11 - Typ. Transfer Characteristics
 $V_{CE} = 50\text{V}$; $t_p = 10\mu\text{s}$**



**Fig. 12 - Typ. Energy Loss vs. I_C
 $T_J = 175^\circ\text{C}$; $L = 200\mu\text{H}$; $V_{CE} = 400\text{V}$; $R_G = 10\Omega$; $V_{GE} = 15\text{V}$**

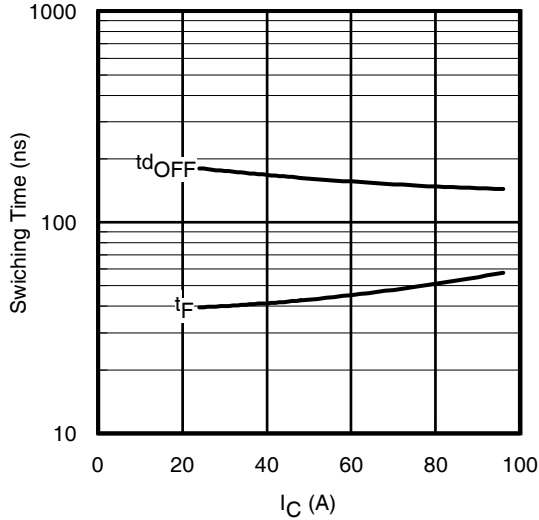


Fig. 13 - Typ. Switching Time vs. I_C
 $T_J = 175^\circ\text{C}$; $L = 200\mu\text{H}$; $V_{CE} = 400\text{V}$; $R_G = 10\Omega$; $V_{GE} = 15\text{V}$

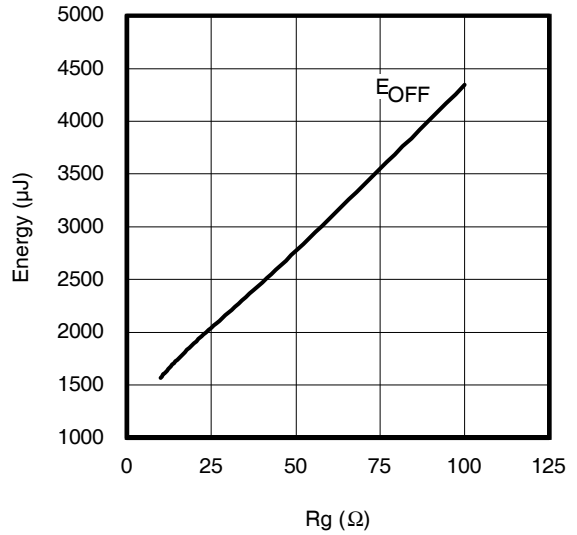


Fig. 14 - Typ. Energy Loss vs. R_G
 $T_J = 175^\circ\text{C}$; $L = 200\mu\text{H}$; $V_{CE} = 400\text{V}$; $I_{CE} = 48\text{A}$; $V_{GE} = 15\text{V}$

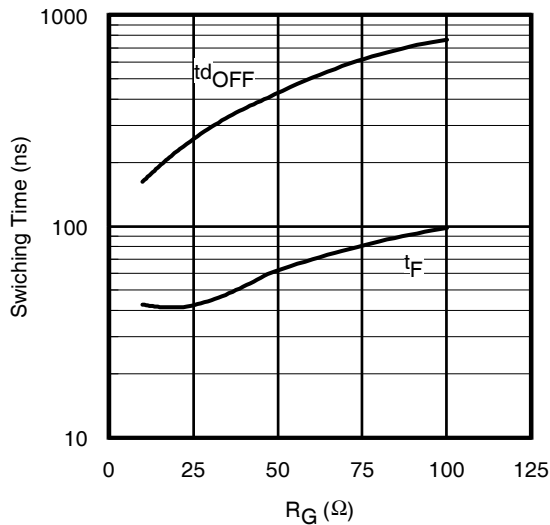


Fig. 15 - Typ. Switching Time vs. R_G
 $T_J = 175^\circ\text{C}$; $L = 200\mu\text{H}$; $V_{CE} = 400\text{V}$; $I_{CE} = 48\text{A}$; $V_{GE} = 15\text{V}$

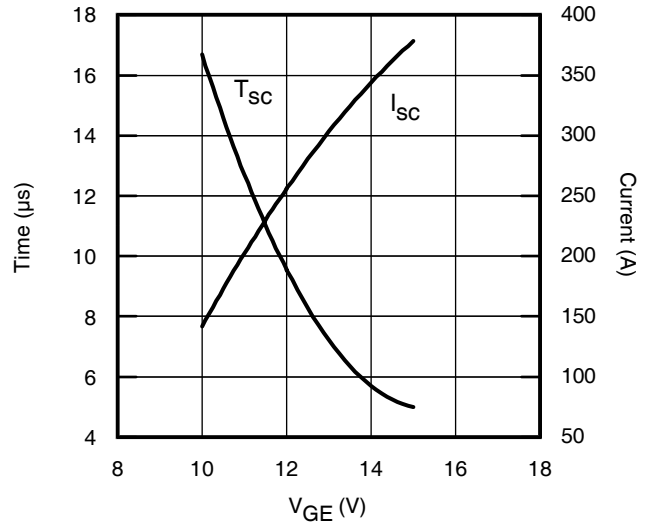


Fig. 16 - V_{GE} vs. Short Circuit
 $V_{CC} = 400\text{V}$; $T_C = 25^\circ\text{C}$

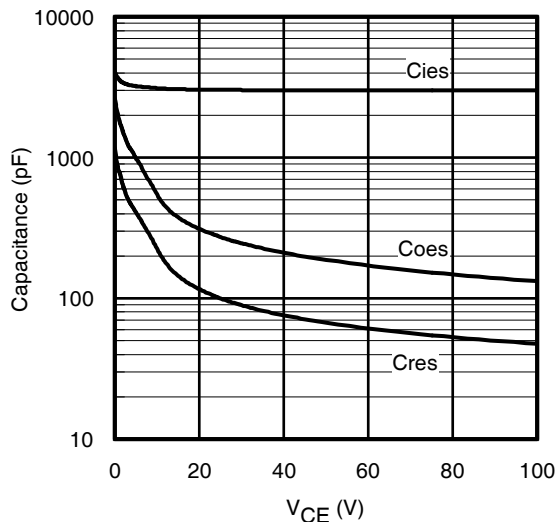


Fig. 17 - Typ. Capacitance vs. V_{CE}
 $V_{GE} = 0\text{V}$; $f = 1\text{MHz}$

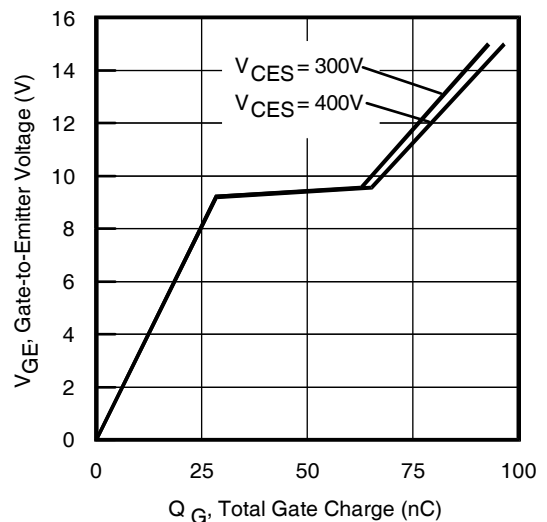


Fig. 18 - Typical Gate Charge vs. V_{GE}
 $I_{CE} = 48\text{A}$; $L = 600\mu\text{H}$

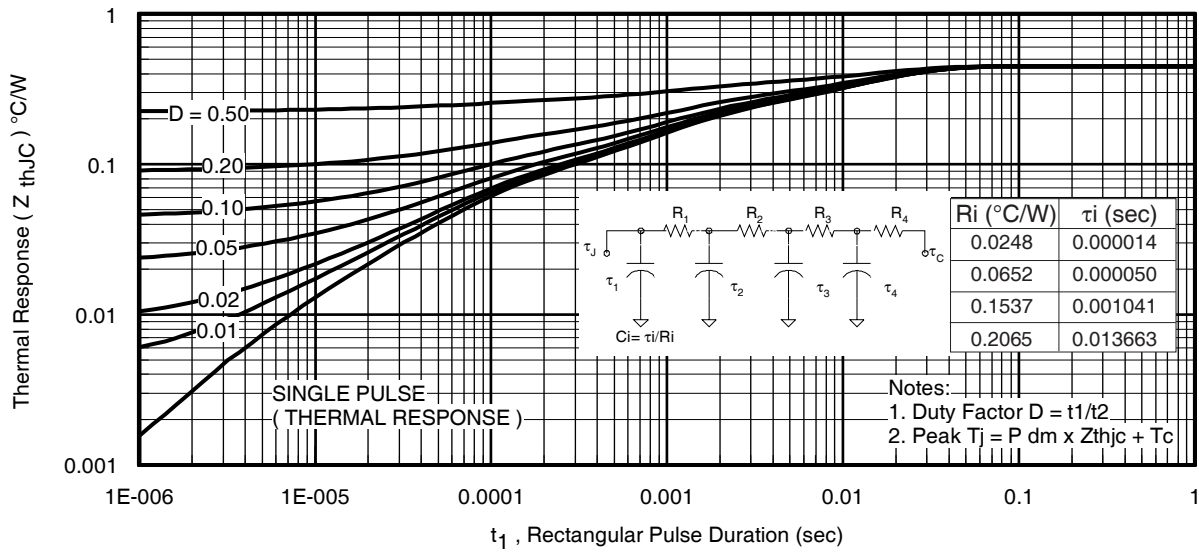


Fig. 19. Maximum Transient Thermal Impedance, Junction-to-Case (IGBT)

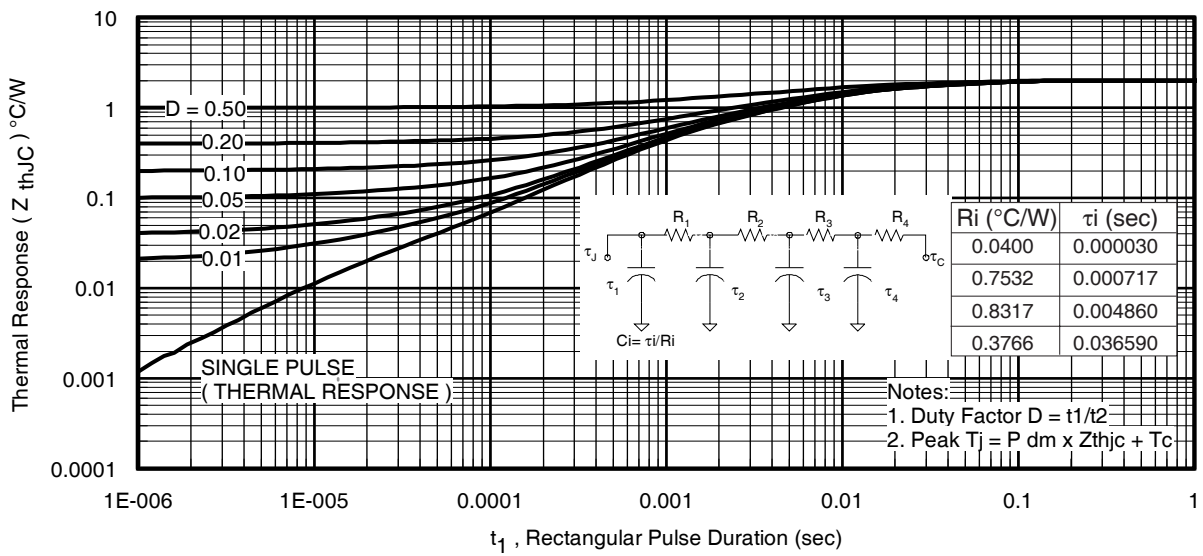


Fig. 20. Maximum Transient Thermal Impedance, Junction-to-Case (DIODE)

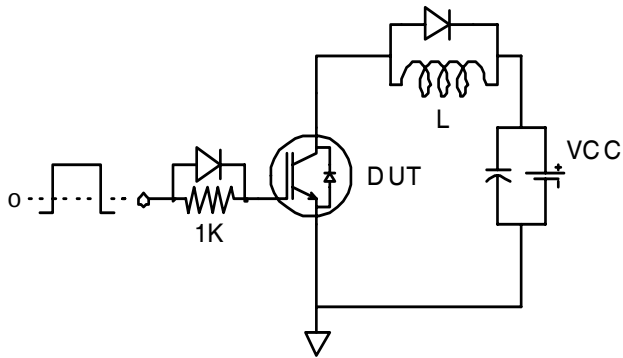


Fig.C.T.1 - Gate Charge Circuit (turn-off)

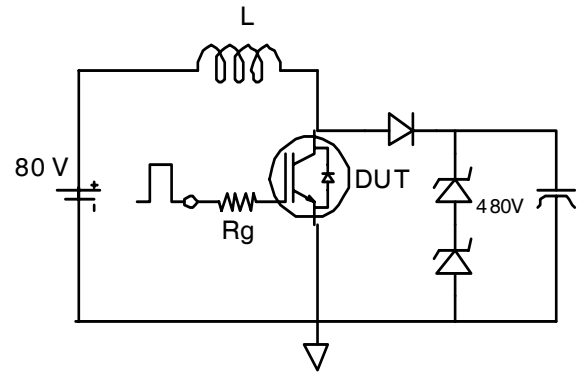


Fig.C.T.2 - RBSOA Circuit

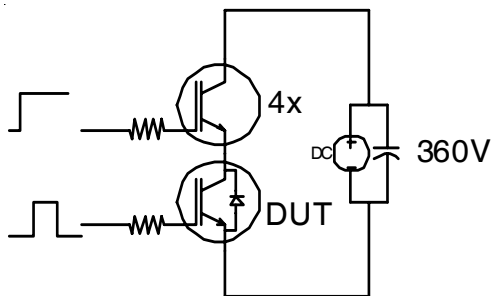


Fig.C.T.3 - S.C. SOA Circuit

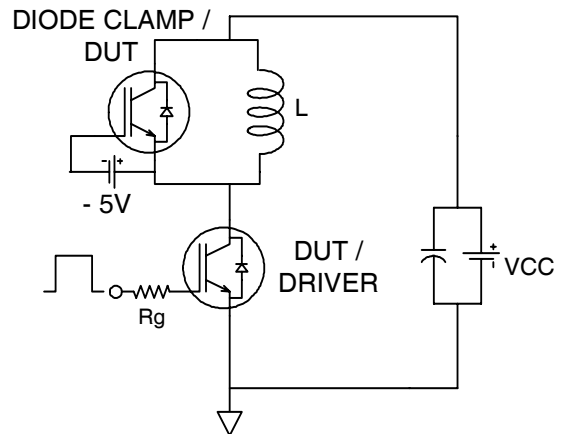


Fig.C.T.4 - Switching Loss Circuit

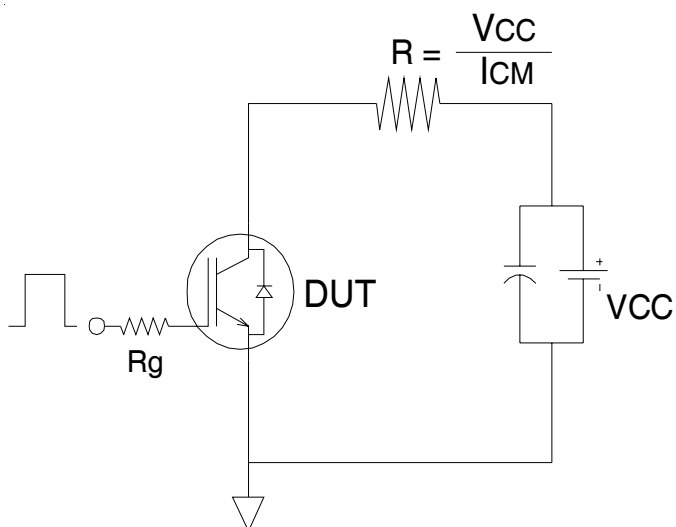


Fig.C.T.5 - Resistive Load Circuit

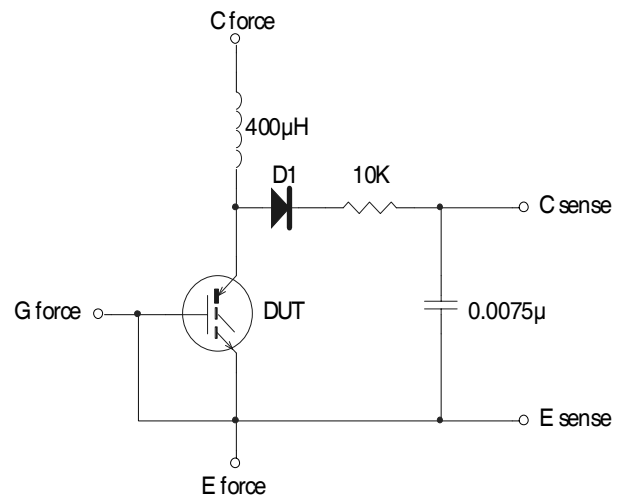


Fig.C.T.6 - BVCES Filter Circuit

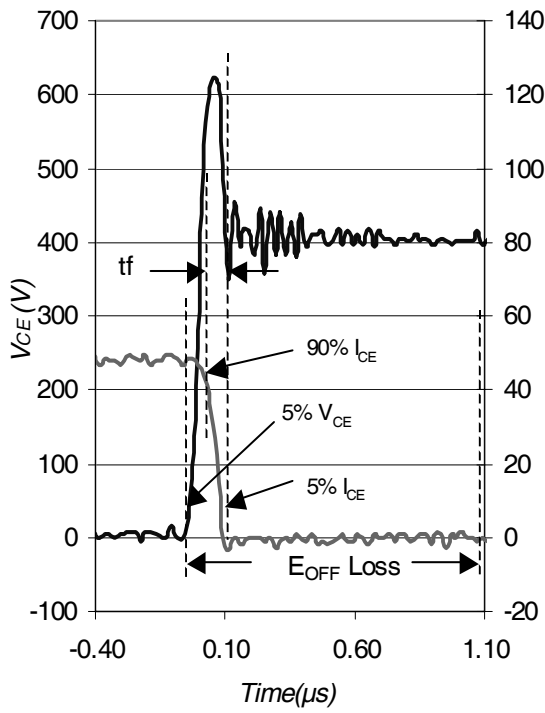


Fig. WF1 - Typ. Turn-off Loss Waveform
@ $T_J = 175^\circ\text{C}$ using Fig. CT.4

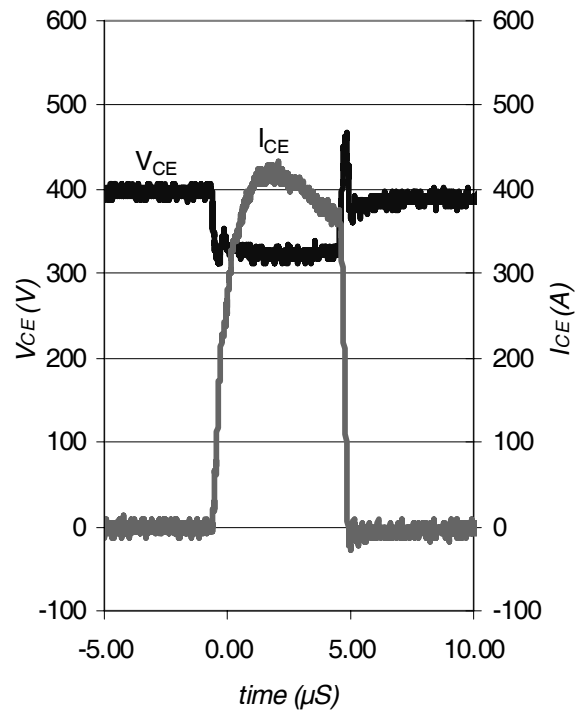
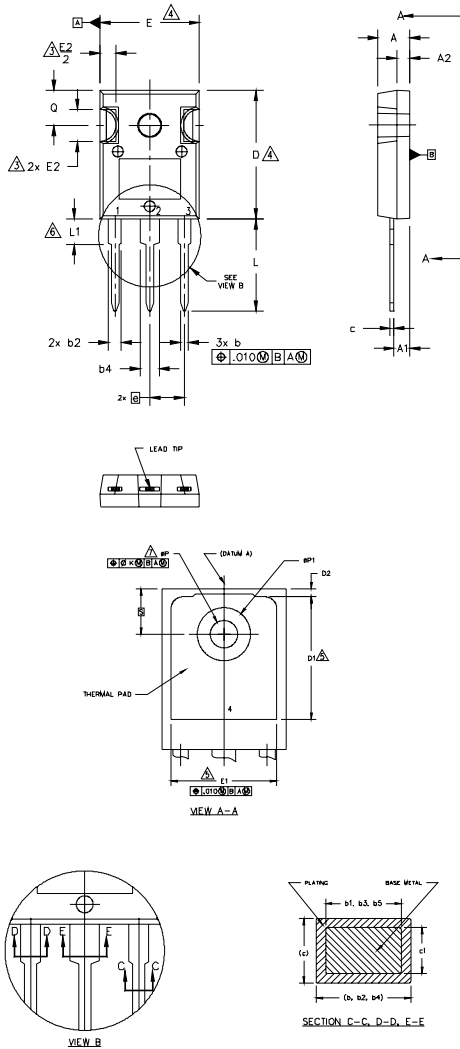


Fig. WF2 - Typ. S.C. Waveform
@ $T_J = 25^\circ\text{C}$ using Fig. CT.3

TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. ØP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	4
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
Øk	.010		0.25		
L	.559	.634	14.20	16.10	
L1	.146	.169	3.71	4.29	
ØP	.140	.144	3.56	3.66	
ØP1	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

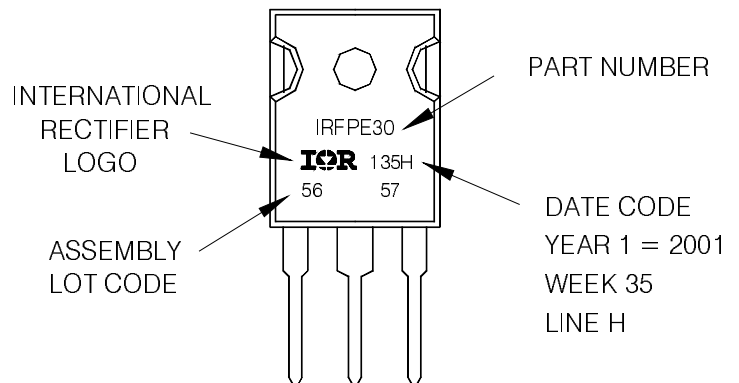
DIODES

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2001
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"

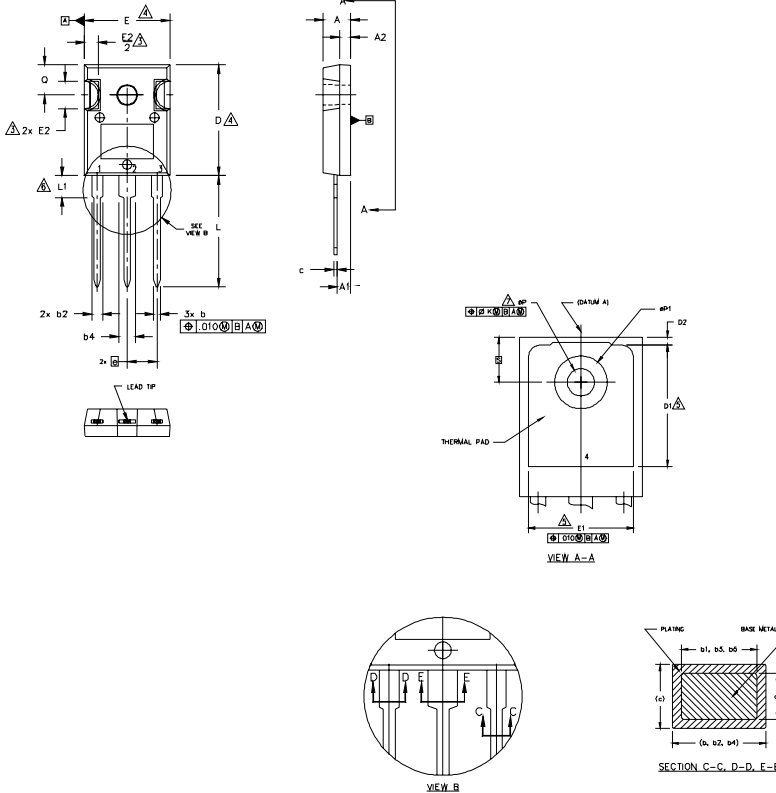


TO-247AC package is not recommended for Surface Mount Application.

IRGP4068DPbF/IRGP4068D-EPbF

TO-247AD Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES.
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7. RP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AD.

SYMBOL	DIMENSIONS				NOTES
	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	.183	.209	4.65	5.31	
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.065	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
c	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	4
D1	.515	-	13.08	-	5
D2	.020	.053	0.51	1.35	4
E	.602	.625	15.29	15.87	
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215 BSC		5.46 BSC		
pk	.010		0.25		
L	.780	.827	19.57	21.00	
L1	.146	.169	3.71	4.29	
ØP	.140	.144	3.56	3.66	
ØP1	-	.291	-	7.39	
Q	.209	.224	5.31	5.69	
S	.217 BSC		5.51 BSC		

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBTs, CoPACK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

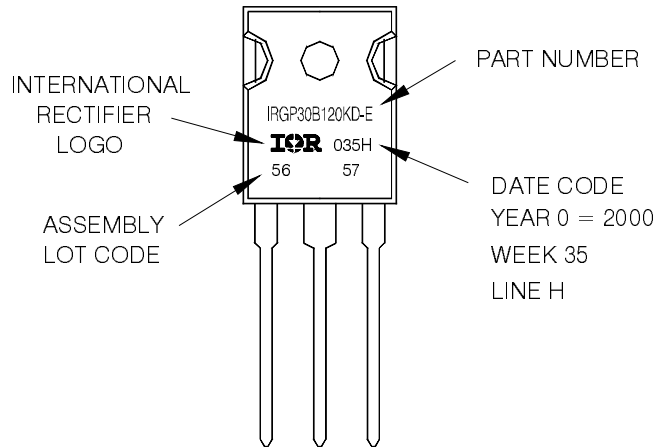
DIODES

- 1.- ANODE/OPEN
- 2.- CATHODE
- 3.- ANODE

TO-247AD Part Marking Information

EXAMPLE: THIS IS AN IRGP30B120KD-E
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2000
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position
indicates "Lead-Free"



TO-247AD package is not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed and qualified for Industrial market.
Qualification Standards can be found on IR's Web site.